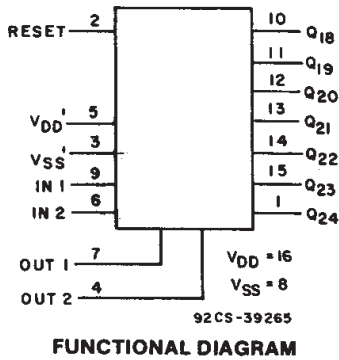


# CD4521B Types

## CMOS 24-Stage Frequency Divider

High-Voltage Types (20-Volt Rating)

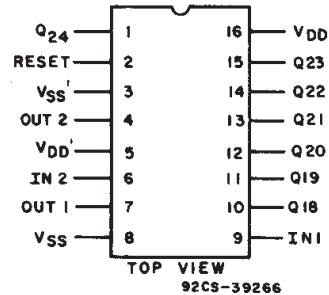


**Features:**

- Reset disables the RC oscillator for low-power standby condition
- VDD' and VSS' pins are brought out from the crystal oscillator to allow use of external resistors for low-power operation
- Maximum input current of 1 µA at 18 V over full package-temperature range: 100 nA at 18 V and 25°C
- Common reset
- 100% tested for 20-V quiescent current
- 5, 10 and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Meets all requirements of JEDEC Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"

■ CD4521B consists of an oscillator section and 24 ripple-carry binary counter stages. The oscillator configuration (using IN1) allows design of either RC or crystal oscillator circuits. IN1 should be tied either HIGH or LOW when not in use. A HIGH on the RESET causes the counter to go to the all-0's state and disables the oscillator. The count is advanced on the negative transition of IN1 (and IN2). A time-saving test mode is described in the Functional Test Sequence Table and in Fig. 6.

The CD4521B types are supplied in 16-lead dual-in-line plastic packages (E suffix), 16-lead small-outline packages (M, M96, MT, and NSR suffixes), and 16-lead thin shrink small-outline packages (PW and PWR suffixes).



**TERMINAL ASSIGNMENT**

OUTPUT	COUNT CAPACITY
Q18	2 <sup>18</sup> = 262,144
Q19	2 <sup>19</sup> = 524,288
Q20	2 <sup>20</sup> = 1,048,576
Q21	2 <sup>21</sup> = 2,097,152
Q22	2 <sup>22</sup> = 4,194,304
Q23	2 <sup>23</sup> = 8,388,608
Q24	2 <sup>24</sup> = 16,777,216

**MAXIMUM RATINGS, Absolute-Maximum Values:**

- DC SUPPLY-VOLTAGE RANGE, (VDD)
  - Voltages referenced to VSS Terminal) ..... -0.5V to +20V
- INPUT VOLTAGE RANGE, ALL INPUTS ..... -0.5V to VDD +0.5V
- DC INPUT CURRENT, ANY ONE INPUT ..... ±10mA
- POWER DISSIPATION PER PACKAGE (PD):
  - For TA = -55°C to +100°C ..... 500mW
  - For TA = +100°C to +125°C ..... Derate Linearly at 12mW/°C to 200mW
- DEVICE DISSIPATION PER OUTPUT TRANSISTOR
  - FOR TA = FULL PACKAGE-TEMPERATURE RANGE (All Package Types) ..... 100mW
- OPERATING-TEMPERATURE RANGE (TA) ..... -55°C to +125°C
- STORAGE TEMPERATURE RANGE (Tstg) ..... -65°C to +150°C
- LEAD TEMPERATURE (DURING SOLDERING):
  - At distance 1/16 ± 1/32 inch (1.59 ± 0.79mm) from case for 10s max ..... +265°C

# CD4521B Types

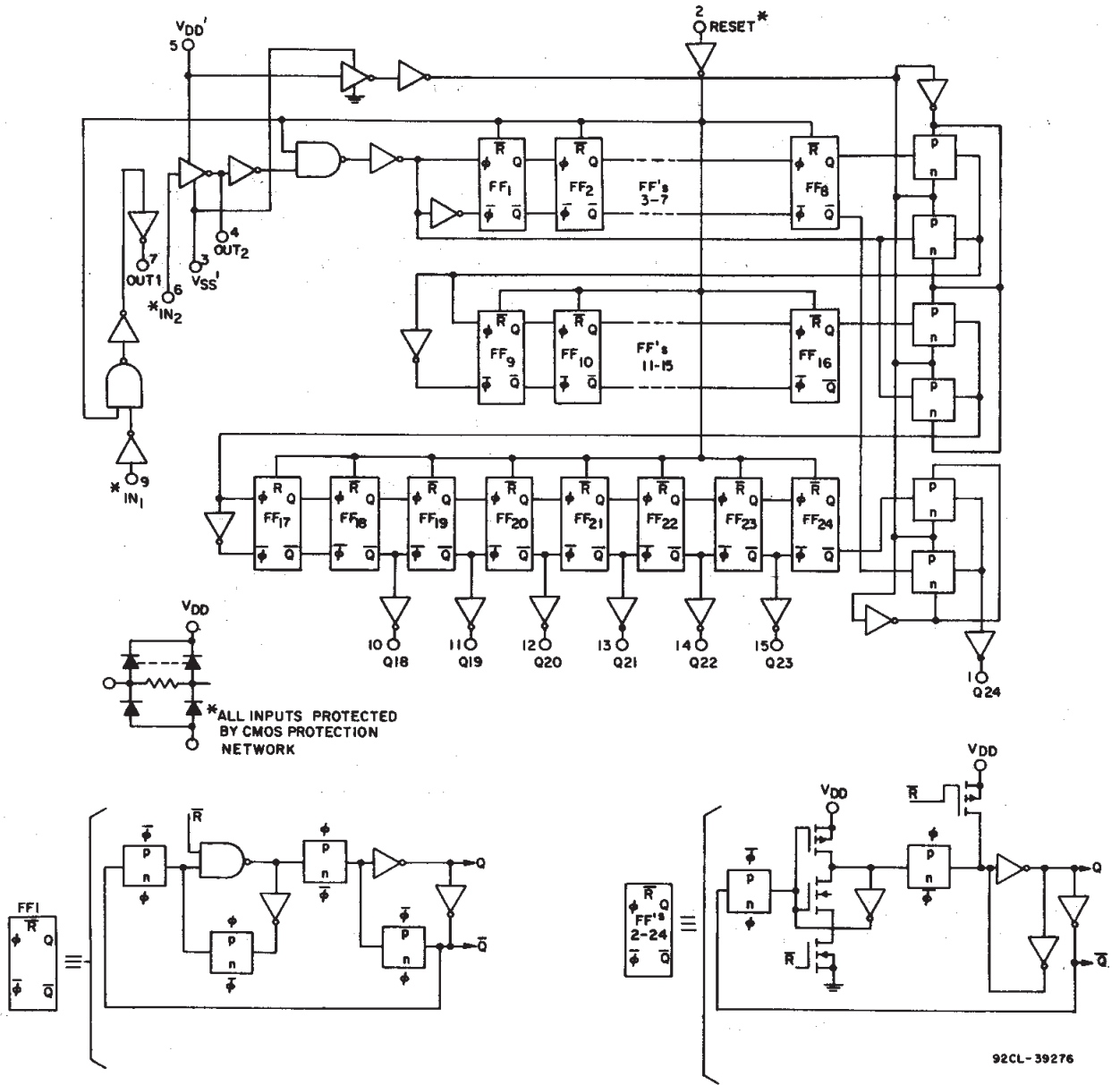


Fig. 1 - Logic diagram for CD4521B.

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## CD4521B Types

### STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I <sub>DD</sub> Max.	—	0, 5	5	5	5	150	150	—	0.04	5	μA
	—	0, 10	10	10	10	300	300	—	0.04	10	
	—	0, 15	15	20	20	600	600	—	0.04	20	
	—	0, 20	20	100	100	3000	3000	—	0.08	100	
Output Low (Sink) Current, I <sub>OL</sub> Min.	0.4	0, 5	5	0.64	0.61	0.42	0.36	0.51	1	—	mA
	0.5	0, 10	10	1.6	1.5	1.1	0.9	1.3	2.6	—	
	1.5	0, 15	15	4.2	4	2.8	2.4	3.4	6.8	—	
Output High (Source) Current, I <sub>OH</sub> Min.	4.6	0, 5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	—	mA
	2.5	0, 5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2	—	
	9.5	0, 10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6	—	
	13.5	0, 15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8	—	
Output Voltage: Low-Level, V <sub>OL</sub> Max.	—	0, 5	5	0.05				—	0	0.05	V
	—	0, 10	10	0.05				—	0	0.05	
	—	0, 15	15	0.05				—	0	0.05	
Output Voltage: High-Level, V <sub>OH</sub> Min.	—	0, 5	5	4.95				4.95	5	—	V
	—	0, 10	10	9.95				9.95	10	—	
	—	0, 15	15	14.95				14.95	15	—	
Input Low Voltage, V <sub>IL</sub> Max.	0.5, 4.5	—	5	1.5				—	—	1.5	V
	1, 9	—	10	3				—	—	3	
	1.5, 13.5	—	15	4				—	—	4	
Input High Voltage, V <sub>IH</sub> Min.	0.5, 4.5	—	5	3.5				3.5	—	—	V
	1, 9	—	10	7				7	—	—	
	1.5, 13.5	—	15	11				11	—	—	
Input Current, I <sub>IN</sub> Max.	—	0, 18	18	±0.1	±0.1	±1	±1	—	±10 <sup>-5</sup>	±0.1	μA

### RECOMMENDED OPERATING CONDITIONS

For maximum reliability, nominal operating conditions should be selected so that operating is always within the following ranges:

CHARACTERISTIC	V <sub>DD</sub> (V)	LIMITS		UNITS
		Min.	Max.	
Supply-Voltage Range (For T <sub>A</sub> = Full Package-Temperature Range)	—	3	18	V
Input Pulse Width	5	340	—	ns
	10	150	—	
	15	120	—	
Reset Pulse Width	5	180	—	ns
	10	80	—	
	15	50	—	
Input Pulse Frequency	5	—	2	MHz
	10	—	5	
	15	—	6.5	
Input Pulse Rise or Fall Time	5	—	15	μs
	10	—	15	
	15	—	15	
R <sub>T</sub> Operating Range	5	1K	10M	Ω
	10	1K	10M	
	15	1K	10M	
C <sub>T</sub> Operating Range	5	15p	10M	F
	10	15p	10M	
	15	15p	10M	

# CD4521B Types

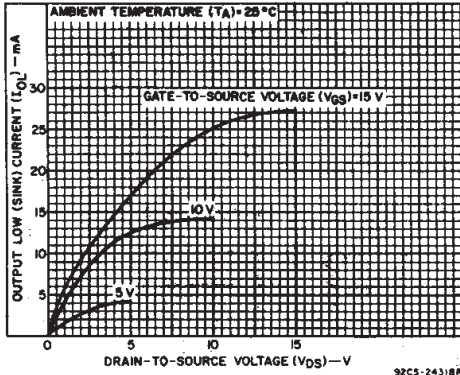


Fig. 2 - Typical output low (sink) current characteristics.

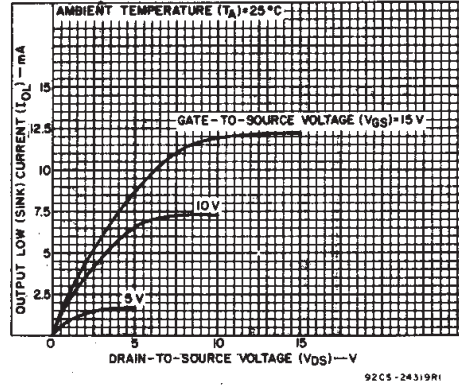


Fig. 3 - Minimum output low (sink) current characteristics.

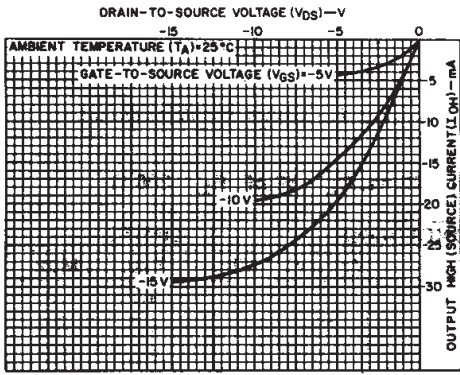


Fig. 4 - Typical output high (source) current characteristics.

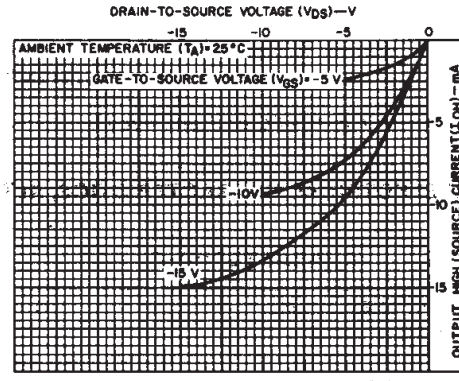


Fig. 5 - Minimum output high (source) current characteristics.

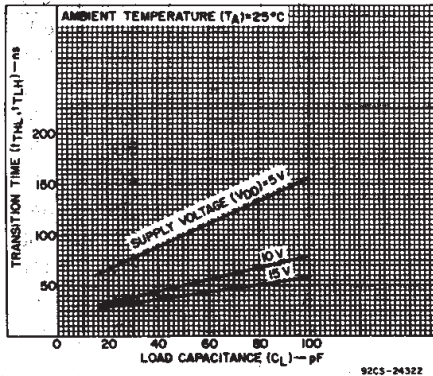


Fig. 6 - Typical transition time as a function of load capacitance.

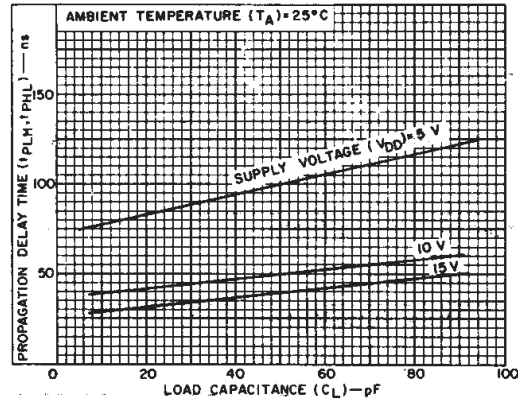


Fig. 7 - Typical propagation delay time ( $Q_n$  to  $Q_{n+1}$ ) as a function of load capacitance.

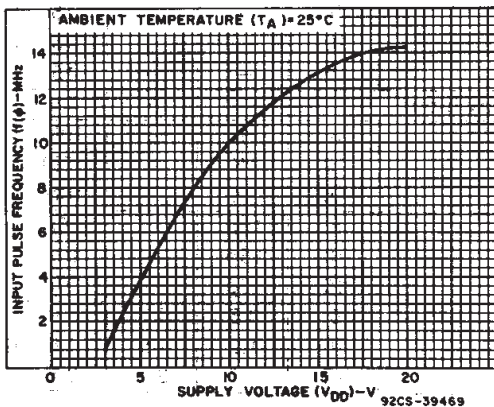


Fig. 8 - Typical maximum input pulse frequency vs. supply voltage.

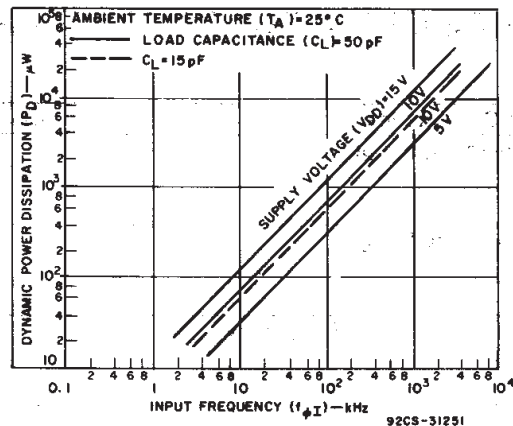


Fig. 9 - Typical dynamic power dissipation as a function of input frequency.

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## CD4521B Types

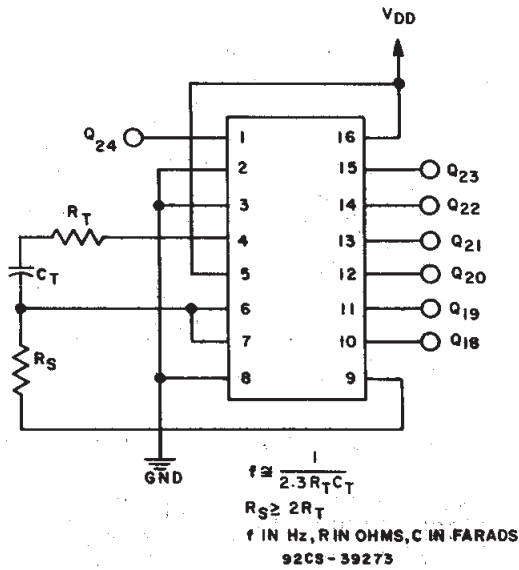


Fig. 10 - RC oscillator circuit.

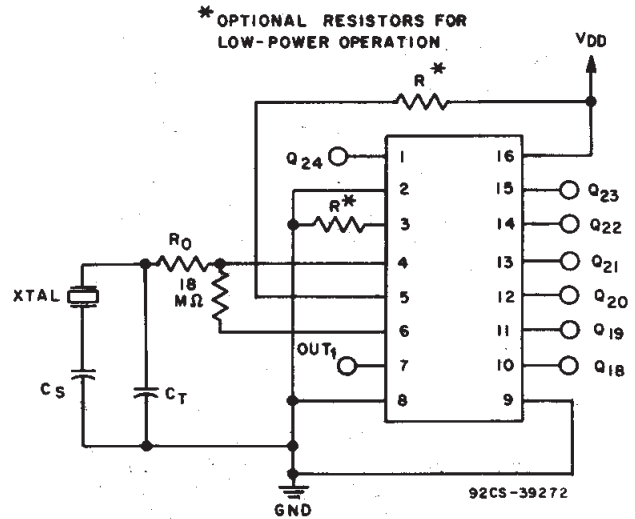


Fig. 11 - Crystal oscillator circuit.

**DYNAMIC ELECTRICAL CHARACTERISTICS, At  $T_A = 25^\circ\text{C}$ ; Input  $t_r, t_f = 20\text{ ns}$ ,  $C_L = 50\text{ pF}$ ,  $R_L = 200\ \Omega$**

CHARACTERISTIC	TEST CONDITIONS	LIMITS			UNITS		
		$V_{DD}(V)$	Min.	Typ.		Max.	
Propagation Delay Time: Input to Q18	$t_{PLH}, t_{PHL}$	5	—	4.5	9	$\mu\text{s}$	
		10	—	1.7	3.5		
		15	—	1.3	2.7		
Input to Q24		5	—	6	12		
		10	—	2.2	4.5		
		15	—	1.7	3.5		
Reset to Qn		5	—	400	800	ns	
		10	—	170	340		
		15	—	120	240		
Transition Time*	$t_{THL}, t_{TLH}$	5	—	100	200		
		10	—	50	100		
		15	—	40	80		
Minimum Input Pulse Width	$t_{w\phi}$	5	—	170	340	ns	
		10	—	75	150		
		15	—	60	120		
Minimum Reset Pulse Width	$t_{w(R)}$	5	—	90	180		ns
		10	—	40	80		
		15	—	25	50		
Maximum Input Pulse Frequency	$f\phi$	5	2	4	—	MHz	
		10	5	10	—		
		15	6.5	13	—		
Input Pulse Rise or Fall Time	$t_r\phi, t_f\phi$	5	—	—	15	$\mu\text{s}$	
		10	—	—	15		
		15	—	—	15		
Input Capacitance	$C_{IN}$	Any Input	—	5	7.5	pF	
$R_T$ Operating Range		5	1K	—	10M	$\Omega$	
		10	1K	—	10M		
		15	1K	—	10M		
$C_T$ Operating Range		5	15p	—	10 $\mu$	F	
		10	15p	—	10 $\mu$		
		15	15p	—	10 $\mu$		
Maximum Oscillator Frequency	$R_T=1\text{ K}\Omega$ $C_T=15\text{ pF}$ $R_S=30\text{ K}\Omega$	5	0.5	0.7	0.9	MHz	
		10	1.2	1.5	1.8		
		15	1.7	2.1	2.5		

\*Not applicable for pin 4 (OUT2).



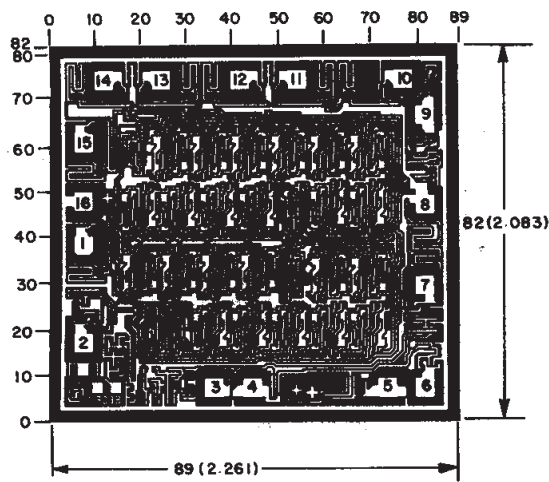
## CD4521B Types

### FUNCTIONAL TEST SEQUENCE

INPUTS		OUTPUTS			Q18-Q24	COMMENTS
RESET	IN 2	OUT 2	V <sub>SS</sub> '	V <sub>DD</sub> '		
1	0	0	V <sub>DD</sub>	V <sub>SS</sub>	LOW	Counter is in three 8-stage sections in parallel mode. Counter is reset. IN 2 and OUT 2 are tied together.
0	1	1	V <sub>DD</sub>	V <sub>SS</sub>		First LOW-to-HIGH transition at IN 2.
0	0	0	V <sub>DD</sub>	V <sub>SS</sub>		255 LOW-to-HIGH transitions are clocked in at IN 2.
	1	1				
	—	—				
	—	—				
0	1	1	V <sub>DD</sub>	V <sub>SS</sub>	HIGH	The 255th LOW-to-HIGH transition.
0	0	0	V <sub>DD</sub>	V <sub>SS</sub>	HIGH	Counter is converted back to 24-stage serial-mode operation.
0	0	0	V <sub>SS</sub>	V <sub>SS</sub>	HIGH	
0	1	0	V <sub>SS</sub>	V <sub>DD</sub>	HIGH	
0	1		V <sub>SS</sub>	V <sub>DD</sub>	HIGH	
0	0		V <sub>SS</sub>	V <sub>DD</sub>	LOW	Counter ripples from an all-HIGH state to an all-LOW state.

A test function, which divides, has been included to reduce the time required to test all 24 stages of the counter. Three sections are loaded in parallel to 255 counts, forcing all the outputs to be in the HIGH state. The counter is changed

back to serial-mode operation and one additional LOW-to-HIGH transition is entered at IN 2, which causes the outputs to ripple from an all-HIGH state to an all-LOW state.



92CS-39275  
Dimensions and pad layout for CD4521BH.

*Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils (10<sup>-3</sup> inch).*

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**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
CD4521BE	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4521BEE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4521BM	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4521BM96	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4521BM96E4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4521BM96G4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4521BME4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4521BMG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4521BMT	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4521BMTE4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4521BMTG4	ACTIVE	SOIC	D	16	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4521BNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4521BNSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4521BPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4521BPWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4521BPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4521BPWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

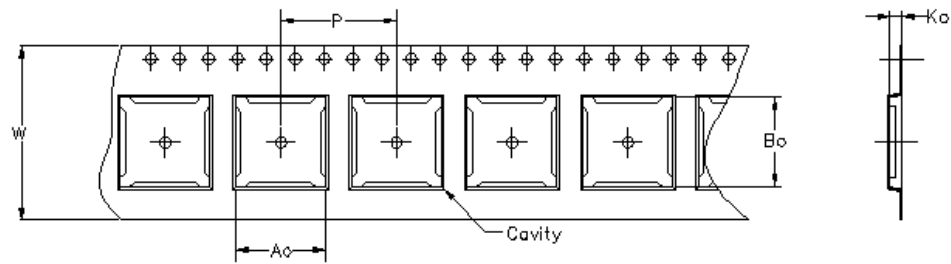
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame

retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

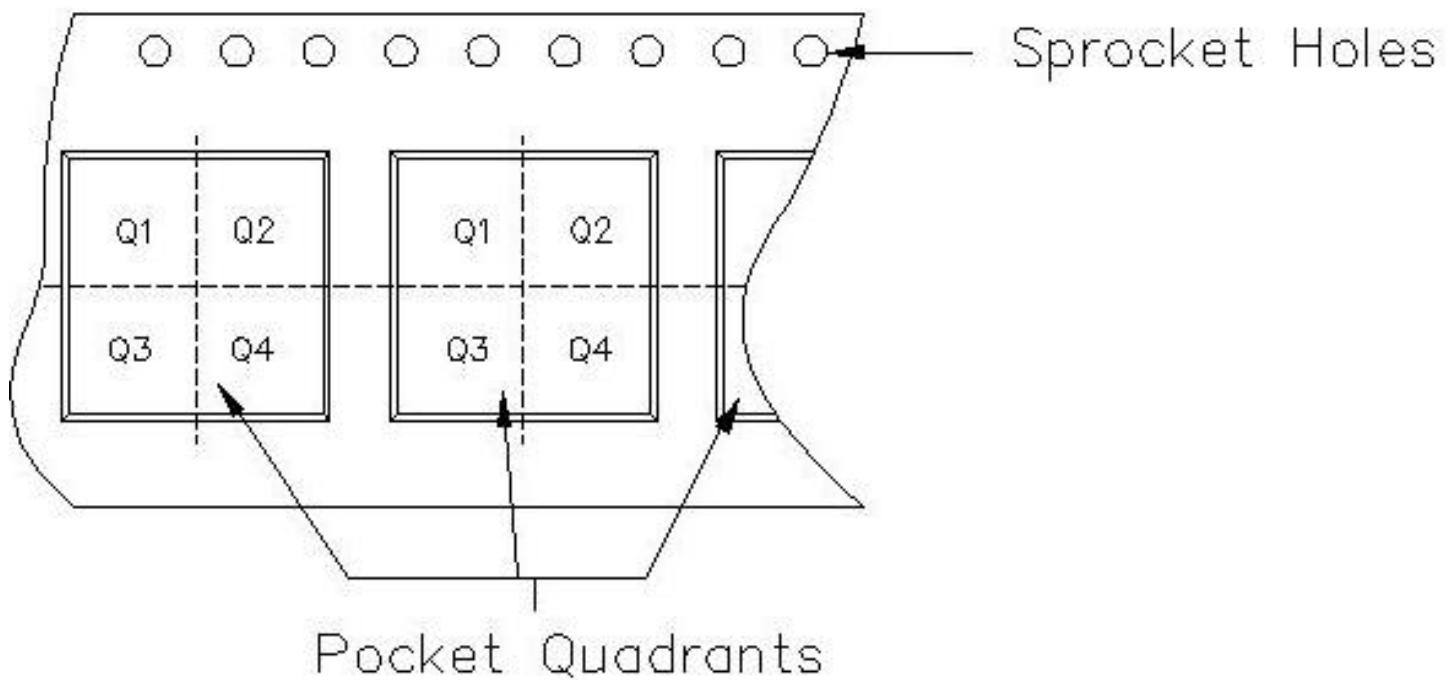
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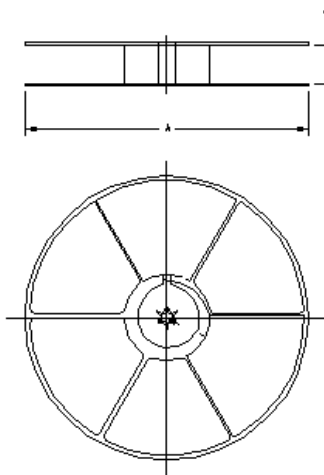
Carrier tape design is defined largely by the component length, width, and thickness.

$A_o$ = Dimension designed to accommodate the component width.
$B_o$ = Dimension designed to accommodate the component length.
$K_o$ = Dimension designed to accommodate the component thickness.
$W$ = Overall width of the carrier tape.
$P$ = Pitch between successive cavity centers.



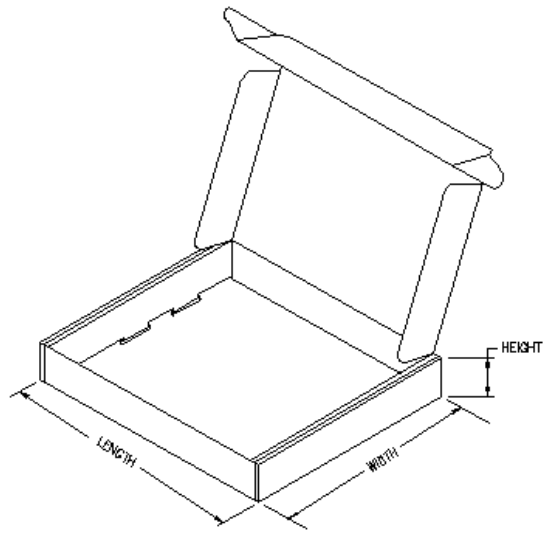
**TAPE AND REEL INFORMATION**

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4521BM96	D	16	FMX	0	16	6.5	10.3	12.1	2	16	Q1
CD4521BNSR	NS	16	MLA	330	16	8.2	10.5	2.5	12	16	Q1
CD4521BPWR	PW	16	MLA	330	12	7.0	5.6	1.6	8	12	Q1



**TAPE AND REEL BOX INFORMATION**

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
CD4521BM96	D	16	FMX	333.2	333.2	28.58
CD4521BNSR	NS	16	MLA	333.2	333.2	28.58
CD4521BPWR	PW	16	MLA	338.1	340.5	20.64



N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D The 20 pin end lead shoulder width is a vendor option, either half or full width.

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## MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.



PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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