

SANYO

No.4688

STK392-020

Convergence Correction Circuit Three Channels in a Single Package (Maximum Output Current : 6A)

Overview

The STK392-020 is a hybrid IC for video projector convergence correction. Since this IC integrates three output amplifier circuits in a single package, the six convergence correction output circuits, i.e., the vertical and horizontal directions for each CRT of the RGB can be formed from only two ICs.

Applications

Video projectors (both standard and high definition)

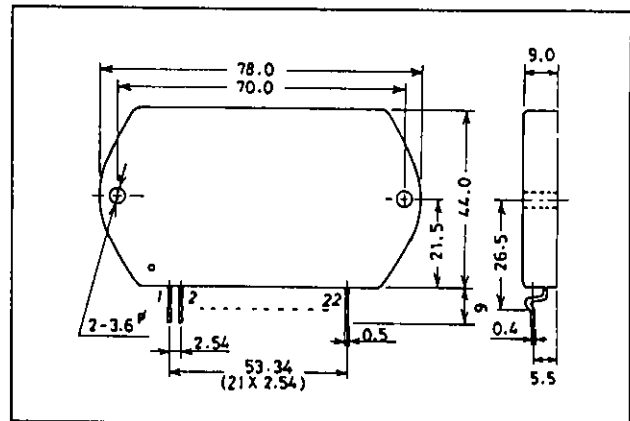
Features

- Three output amplifier circuits integrated in a single 22-pin package
- High absolute maximum supply voltage ($V_{CC \text{ max}} = \pm 44 \text{ V}$)
- Low thermal resistance ($\theta_{j-c} = 2.1 \text{ }^\circ\text{C/W}$)
- High thermal stability ($T_C \text{ max} = 125^\circ\text{C}$)
- Isolated early stage and output stage power supplies
- Output stage power supply switching supports high efficiency designs.
- The input system, power supply system and output system pins are isolated in the pin arrangement, thus reducing the influence of the pattern layout on the characteristics and easing design.
- Since constant current circuits are used in the pre-driver stage, operation is stable with respect to the power supply switching.
- The Sanyo convergence correction circuit product lineup (the STK392-000 series) handles a wide range of end-product classes. Therefore, the same PCB can be used for end products from popularly-priced units to top-of-the-line models.

Package Dimensions

unit: mm

4086A



Specifications

Absolute Maximum Ratings at $T_a = 25^\circ\text{C}$

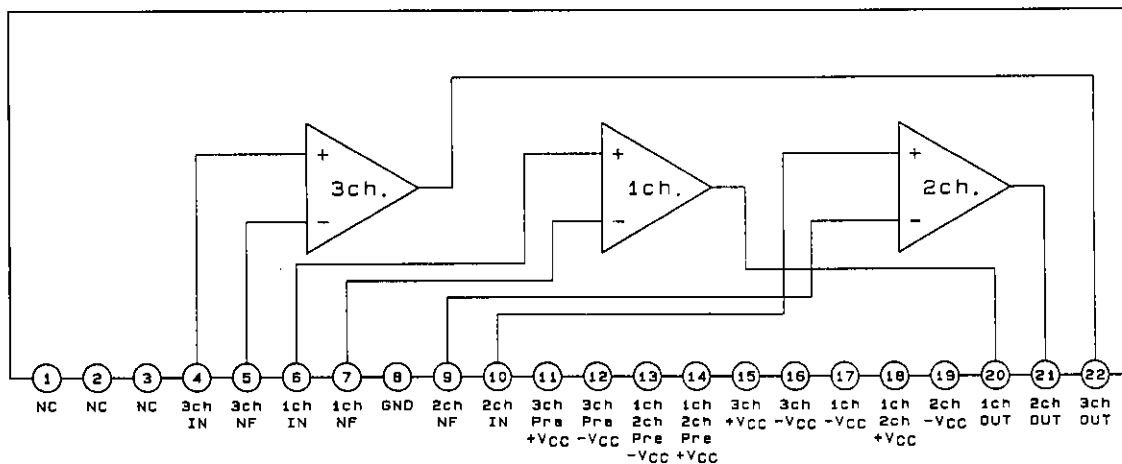
Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	$V_{CC \text{ max}}$		± 44	V
Maximum collector current	I_C	Tr8, 10, 18, 20, 28, 30	+6.0	A
Thermal resistance	θ_{j-c}	Tr8, 10, 18, 20, 28, 30 (per transistor)	2.1	$^\circ\text{C/W}$
Junction temperature	T_j		150	$^\circ\text{C}$
Operating substrate temperature	T_c		125	$^\circ\text{C}$
Storage temperature	T_{stg}		-30 to +125	$^\circ\text{C}$

SANYO Electric Co., Ltd. Semiconductor Business Headquarters
TOKYO OFFICE Tokyo Bldg., 1-10, 1 Chome, Ueno, Taito-ku, TOKYO, 110 JAPAN

Operating Characteristics at $T_a = 25^\circ\text{C}$, $R_g = 50 \Omega$

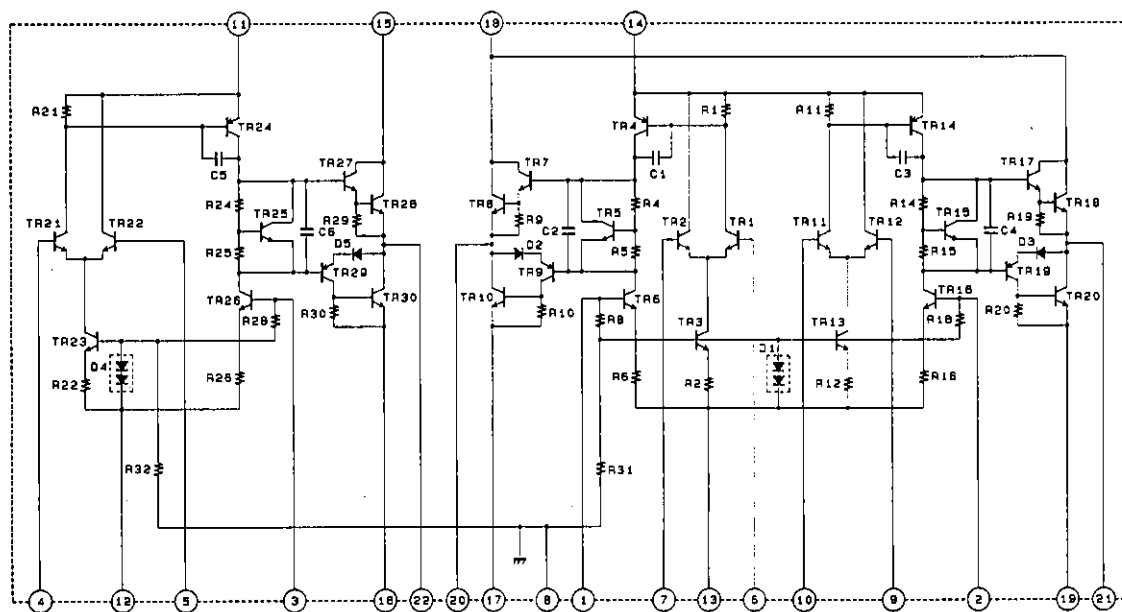
Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
Output noise voltage	V_{NO}	$V_{CC} = \pm 35 \text{ V}$			0.2	mVrms
Quiescent current	I_{CCO}	$V_{CC} = \pm 35 \text{ V}$	30	90	150	mA
Neutral voltage	V_N	$V_{CC} = \pm 35 \text{ V}$	-50	0	+50	mV
Output delay time	t_D	$V_{CC} = \pm 35 \text{ V}$, $f = 15.75 \text{ kHz}$; Triangle wave input, $V_{OUT} = 1.5 \text{ V}_{p-p}$			1.0	μs

Equivalent Circuit Block Diagram



A01699

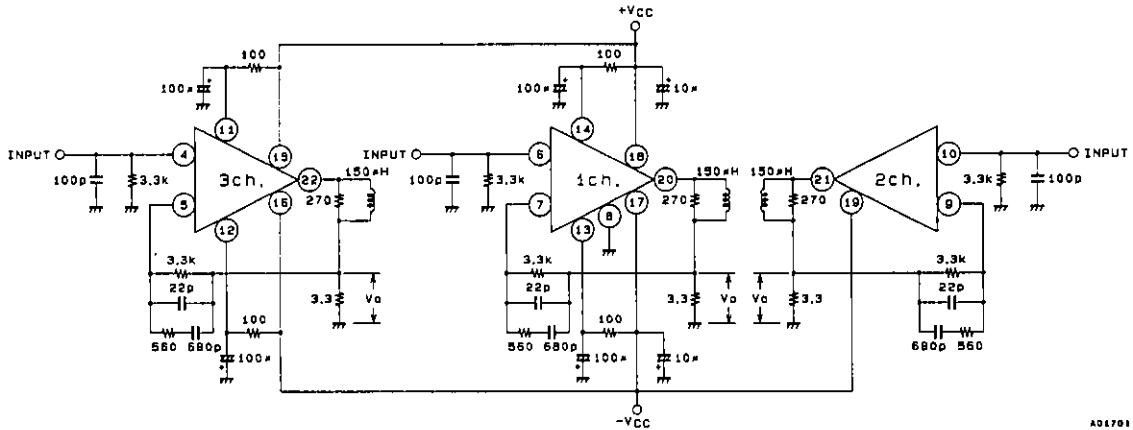
Internal Equivalent Circuit



A01700

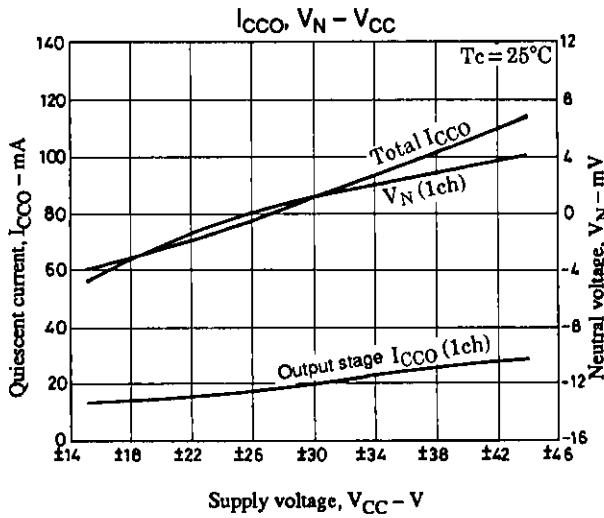
Test Circuit

Unit (Resistance: Ω, Capacitance: F)

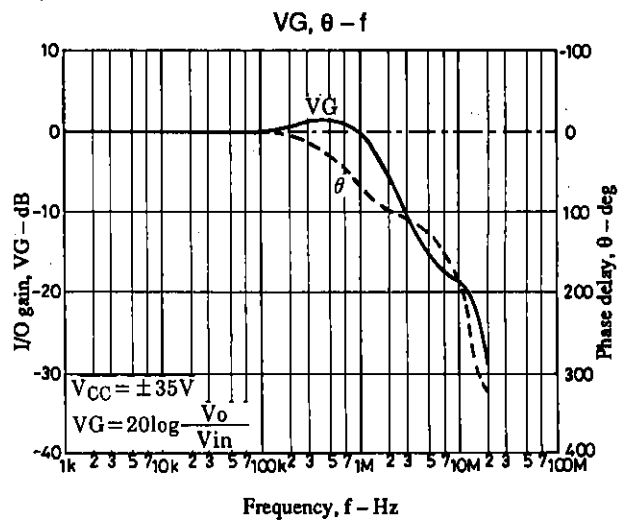
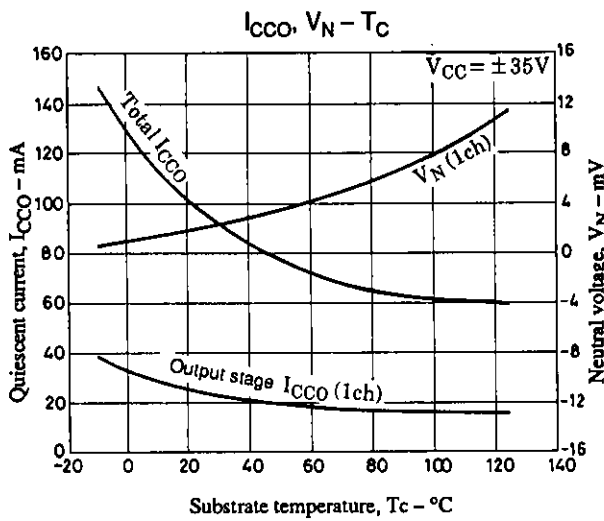
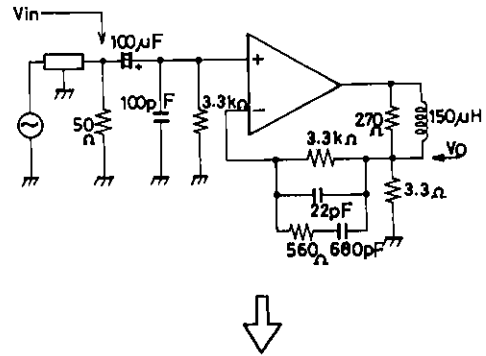


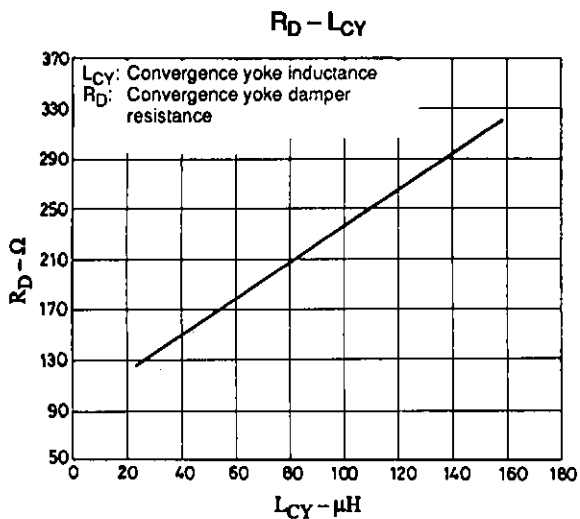
A06701

Vo: Connect to VTVM when measuring V_{NO}
 Connect to a DC volt meter when measuring V_N
 Connect to the oscilloscope when measuring t_D

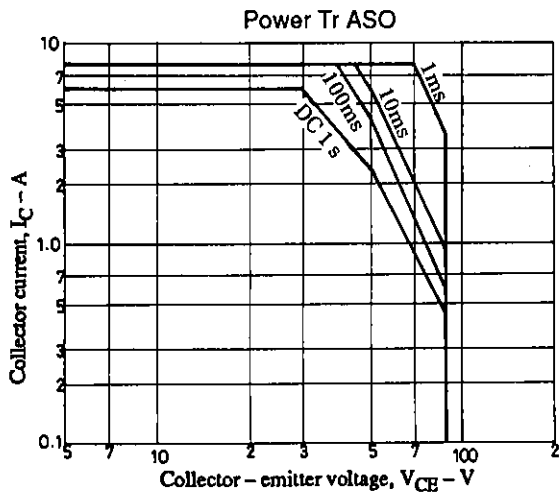
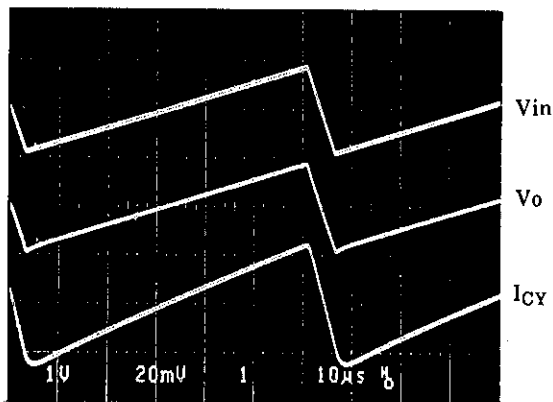
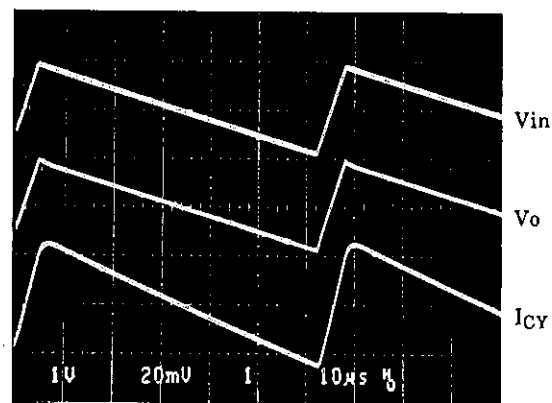
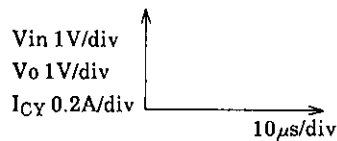
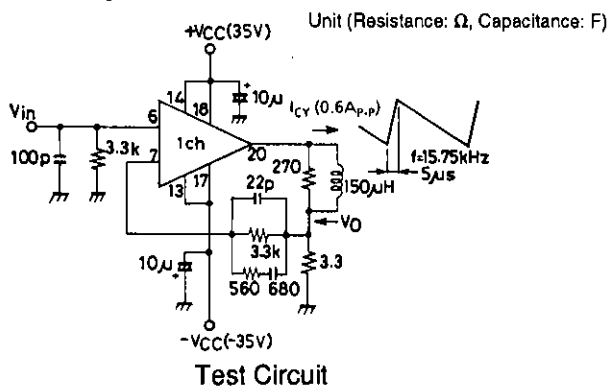


Test Circuit





Operating Waveforms



Thermal Design

1. T_j max, T_c max, and θ_{j-c}

T_j max, T_c max, and θ_{j-c} are stipulated in the maximum ratings as required parameters for thermal design.

- T_j max (junction temperature)

T_j max is a parameter that is due to the physical structure of the internal devices. Since devices will be degraded or destroyed if T_j exceeds this value, the design must not allow this value to be exceeded.

- T_c max (operating substrate temperature)

T_c max is a parameter that arises from the internal devices, the materials used, and the circuit design. It is determined based on comprehensive considerations, including reliability. Devices are not guaranteed if they are operated with T_c exceeding this value.

- θ_{j-c} (thermal resistance)

θ_{j-c} differs for each device in the design, and is stipulated in the maximum ratings since it is required to calculate T_j for the major devices in the design.

Note that T_j and T_c are independent parameters that depend on the operating conditions, and the thermal design must fulfill the maximum ratings of both these parameters.

2. Approaches to Thermal Design

Let P_d be the IC case internal operating power dissipation, and P_c be the power dissipation per power transistor. The required heat sink thermal resistance (θ_{c-a}) for this case internal power dissipation (P_d) can be derived as follows:

Condition 1: Taking T_a to be the end product guaranteed ambient temperature, the IC case temperature T_c must not exceed 125°C.

$$P_d \times \theta_{c-a} + T_a < 125^\circ\text{C} \text{ (} T_c \text{ max)} \dots\dots\dots \textcircled{1}$$

Condition 2: The power transistor junction temperature must not exceed 150°C.

$$P_d \times \theta_{c-a} + P_c \times \theta_{j-c} + T_a < 150^\circ\text{C} \text{ (} T_j \text{ max)} \dots\dots\dots \textcircled{2}$$

Where θ_{j-c} is the thermal resistance per power transistor.

The thermal design must fulfill these above conditions.

3. Design Procedure

The figure at right shows a model of the STK392-020 channel 1 circuit. Taking the P_d 's of each channel to be P_{d1} (channel 1), P_{d2} (channel 2) and P_{d3} (channel 3), the total P_d max can be determined as:

$$P_d \text{ max} = P_{d1} \text{ max} + P_{d2} \text{ max} + P_{d3} \text{ max}$$

That is, condition ① gives:

$$\theta_{c-a} < \frac{T_c \text{ max} - T_a \text{ max}}{P_d \text{ max}} \dots\dots\dots \textcircled{3}$$

which allows the required heat sink thermal resistance to be derived.

(Here, T_c max is taken to be 125°C.)

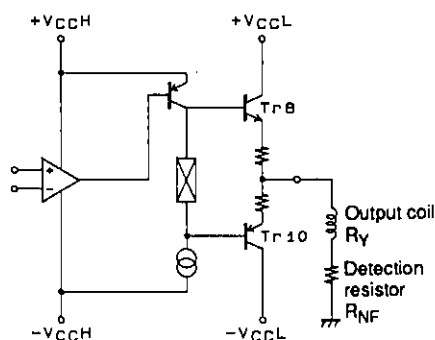
Also, taking the power dissipation per power transistor for each channel to be P_c , the transistor junction temperature T_j will be:

$$T_j = P_d \text{ max} \times \theta_{c-a} + T_a + P_c \times \theta_{j-c} \dots\dots\dots \textcircled{4}$$

and this can be used to confirm that T_j does not exceed T_j max (150°C).

At this point, if T_j exceeds 150°C in the design, T_c must be lowered by lowering the heat sink thermal resistance θ_{c-a} so that T_j does not exceed 150°C.

STK392-020 Circuit Model (channel 1)



A01702

4. Thermal Design Example

Take the following to be the worst operating conditions for the STK392-020.

$$V_{CCH} = \pm 35 \text{ V}$$

$$V_{CCL} = \pm 25 \text{ V}$$

Output coil, $L_Y = 150 \mu\text{H}$, $R_Y = 0 \Omega$

Current detection resistor $R_{NF} = 3.3 \Omega$

$I_{p-o} \text{ max} = 0.4 \text{ A}$, $I_{p-p} = 0.8 \text{ A}$, Sawtooth waveform input

$I_{o(\text{DC})} \text{ max} = 0.4 \text{ A}$ DC input

All three channels operating under the same conditions

$T_a \text{ max} = 60^\circ\text{C}$ (unit internal temperature)

From figures 1 and 2, it can be seen that the Pd1 for channel 1 is:

(a) For a sawtooth wave input: Pd1 max = 4.8 W (AC)

(b) For a DC input: Pd1 max = 9.5 W (DC)

This shows that Pd1 max AC < Pd1 max DC, i.e. that Pd1 is larger for a DC input.

Also, considering Pc for the output transistors gives:

(a) For a sawtooth wave (AC) input: Pc = 1/2 Pd1

(b) For a DC input: Pc = Pd1 (Since the power concentrates in the transistor on one side.)

Therefore, the DC input Pc for the output transistors is larger.

Accordingly, the remainder of the thermal design is based on the DC input case.

Here we ignore the power dissipation in the early stages.

When: Pd1 max = Pd2 max = Pd3 max = 9.5 W, then the Pd max (total for three channels) will be:

$$Pd \text{ max} = Pd1 \text{ max} \times 3 = 28.5 \text{ W}$$

$$\theta_{c-a} = \frac{T_c \text{ max} - T_a}{Pd \text{ max}} = \frac{125 - 60}{28.5} = 2.28^\circ\text{C/W}$$

This means that if a 2 mm thick Al plate (with an unfinished surface) is used as the heat sink, then figure 3 shows that the following area S is required.

$$S = 625 \text{ cm}^2 (25 \times 25 \text{ cm})$$

Also, from formula ④, we see that the power transistor junction temperature Tj at this time will be:

$$\begin{aligned} T_j &= Pd \text{ max} \times \theta_{c-a} + T_a + Pc \text{ max} \times \theta_{j-c} \\ &= 28.5 \times 2.28 + 60 + 9.5 \times 2.1 \\ &= 145^\circ\text{C} \end{aligned}$$

This is a 5°C derating from the required 150°C Tj max.

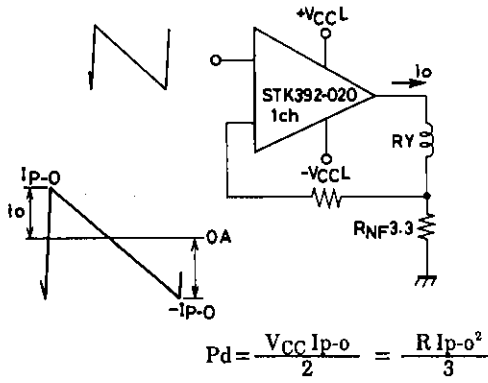
(Addendum) To be precise, the power dissipated in the early stage circuits (transistor, resistors, etc.) should also be taken into consideration.

Figure 1: Sawtooth wave input (AC) I_{p-o} – Pd1

Figure 2: DC input $I_{o(\text{DC})}$ – Pd1

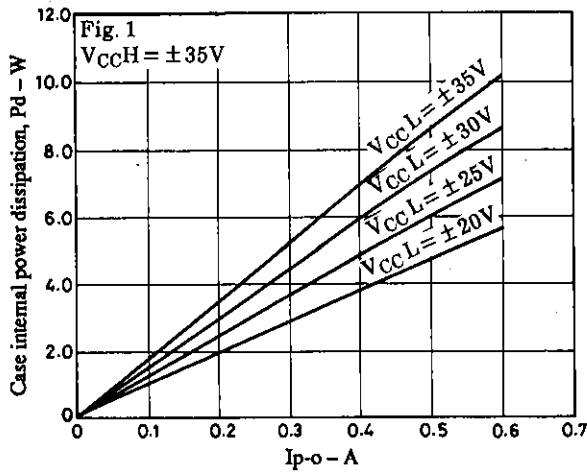
Figure 3: Aluminum plate thermal resistance characteristics

Sawtooth wave Input

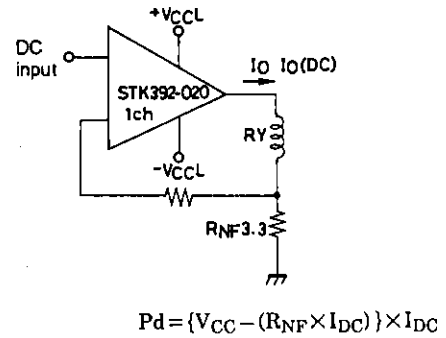


$(R = R_{NF} + R_Y \approx R_{NF})$

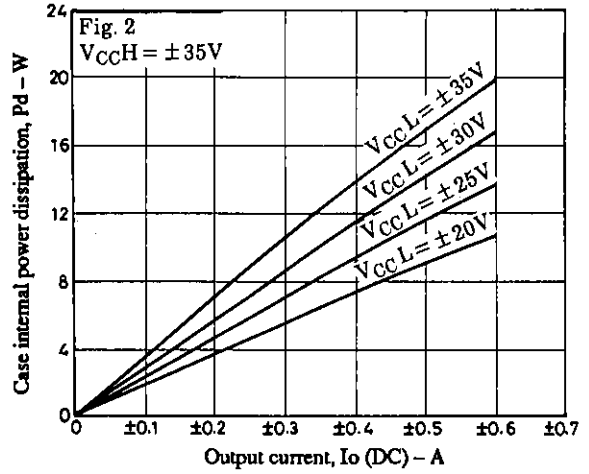
↓
Pd - Ip-o



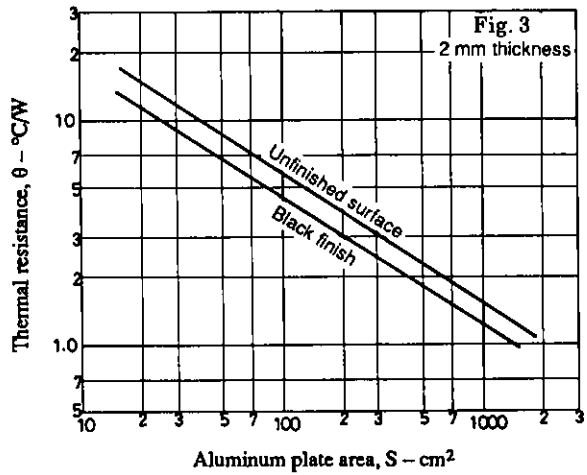
DC Input



↓
Pd - Io



Aluminum plate thermal resistance



- No products described or contained herein are intended for use in surgical implants, life-support systems, aerospace equipment, nuclear power control systems, vehicles, disaster/crime-prevention equipment and the like, the failure of which may directly or indirectly cause injury, death or property loss.
- Anyone purchasing any products described or contained herein for an above-mentioned use shall:
 - ① Accept full responsibility and indemnify and defend SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors and all their officers and employees, jointly and severally, against any and all claims and litigation and all damages, cost and expenses associated with such use;
 - ② Not impose any responsibility for any fault or negligence which may be cited in any such claim or litigation on SANYO ELECTRIC CO., LTD., its affiliates, subsidiaries and distributors or any of their officers and employees jointly or severally.
- Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. SANYO believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.

This catalog provides information as of **June , 1996** . Specifications and information herein are subject to change without notice.