

Silicon PNP Power Transistors

2SA885

DESCRIPTION

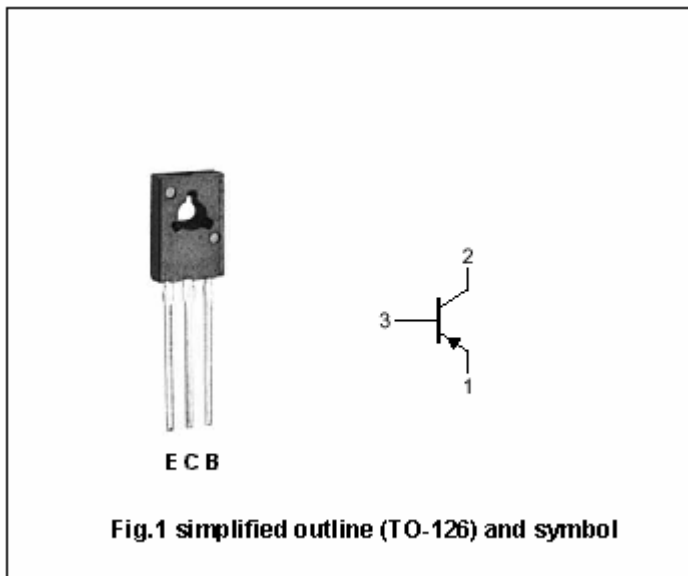
- With TO-126 package
- Complement to type 2SC1846
- Low collector-emitter saturation voltage

APPLICATIONS

- For low-frequency power amplification

PINNING

PIN	DESCRIPTION
1	Emitter
2	Collector;connected to mounting base
3	Base



Absolute Maximun Ratings (Ta=25 )

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V <sub>CBO</sub>	Collector-base voltage	Open emitter	-45	V
V <sub>CEO</sub>	Collector-emitter voltage	Open base	-35	V
V <sub>EBO</sub>	Emitter-base voltage	Open collector	-5	V
I <sub>C</sub>	Collector current (DC)		-1	A
I <sub>CM</sub>	Collector current-peak		-1.5	A
P <sub>C</sub>	Collector power dissipation	T <sub>C</sub> =25	1.2* <sup>1</sup>	W
			5* <sup>2</sup>	
T <sub>j</sub>	Junction temperature		150	
T <sub>stg</sub>	Storage temperature		-55~150	

Note) \*1: Without heat sink

\*2: With a 100 × 100 × 2 mm A1 heat sink

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## CHARACTERISTICS

T<sub>j</sub>=25 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V <sub>(BR)CEO</sub>	Collector-emitter breakdown voltage	I <sub>C</sub> =-2mA; I <sub>B</sub> =0	-35			V
V <sub>(BR)CBO</sub>	Collector-base breakdown voltage	I <sub>C</sub> =-10 μ A ; I <sub>E</sub> =0	-45			V
V <sub>CEsat</sub>	Collector-emitter saturation voltage	I <sub>C</sub> =-0.5A ; I <sub>B</sub> =-50mA			-0.5	V
I <sub>CBO</sub>	Collector cut-off current	V <sub>CB</sub> =-20V; I <sub>E</sub> =0			-0.1	μ A
I <sub>CEO</sub>	Collector cut-off current	V <sub>CE</sub> =-20V; I <sub>B</sub> =0			-100	μ A
I <sub>EBO</sub>	Emitter cut-off current	V <sub>EB</sub> =-5V; I <sub>C</sub> =0			-10	μ A
h <sub>FE-1</sub>	DC current gain	I <sub>C</sub> =-0.5A ; V <sub>CE</sub> =-10V	85		340	
h <sub>FE-2</sub>	DC current gain	I <sub>C</sub> =-1A ; V <sub>CE</sub> =-5V	50			
C <sub>OB</sub>	Output capacitance	I <sub>E</sub> =0 ; V <sub>CB</sub> =-10V; f=1MHz		20	30	pF
f <sub>T</sub>	Transition frequency	I <sub>C</sub> =50mA ; V <sub>CB</sub> =-10V; f=200MHz		200		MHz

◆ h<sub>FE-1</sub> Classifications

Q	R	S
85-170	120-240	170-340

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PACKAGE OUTLINE

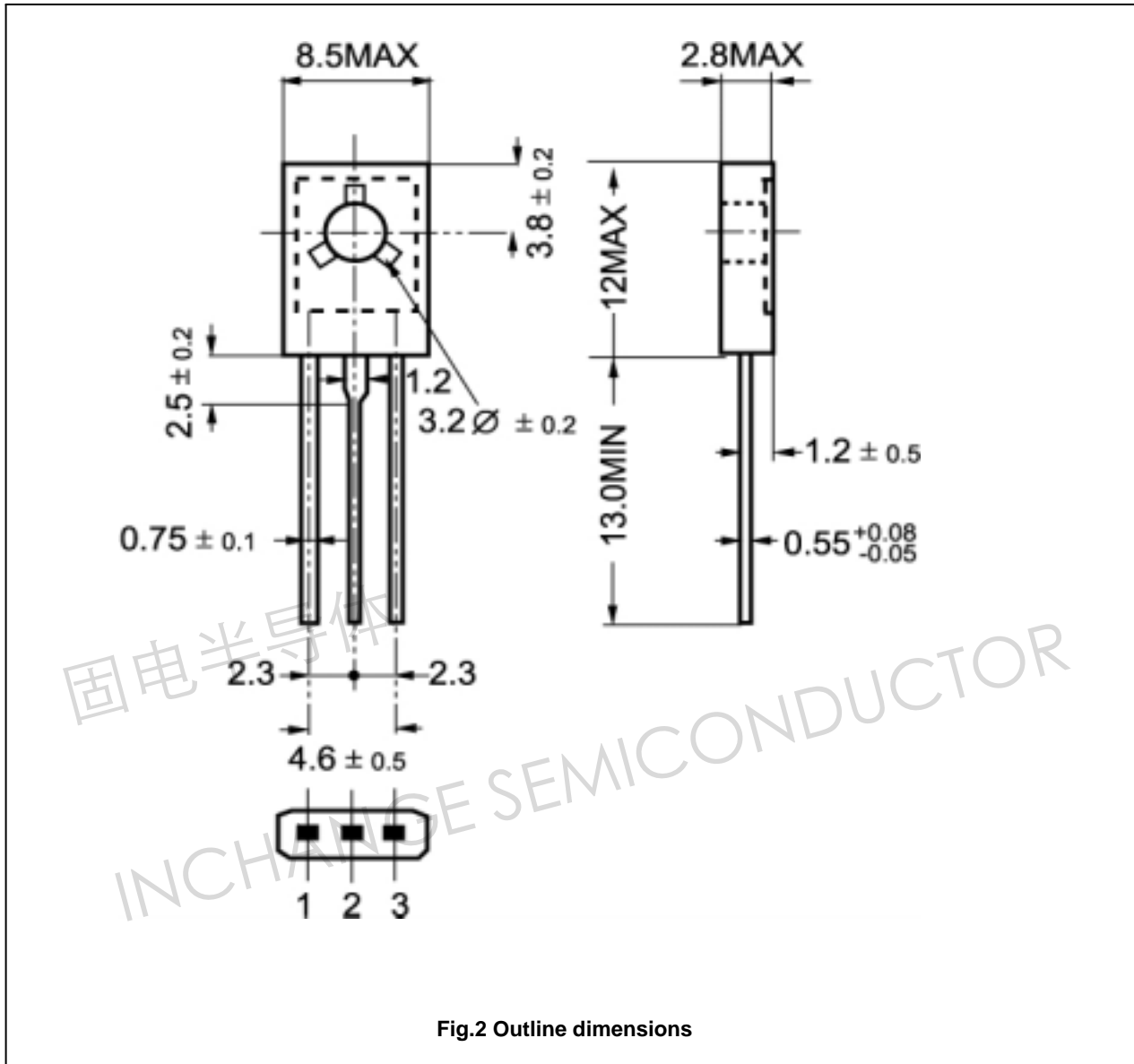


Fig.2 Outline dimensions

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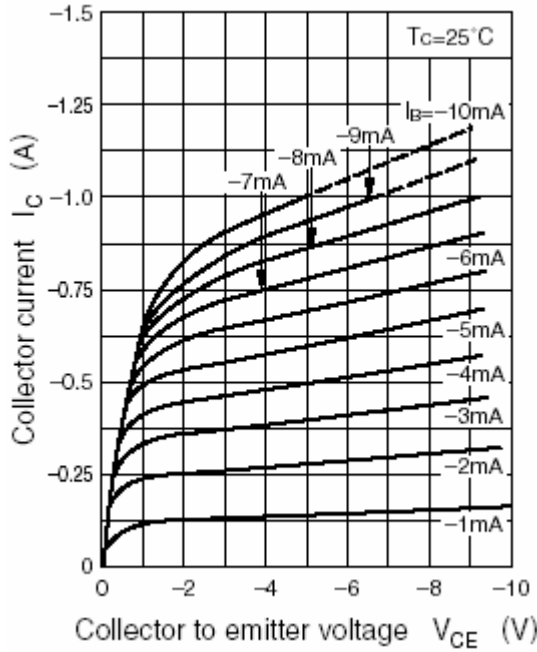


Fig.3 Static Characteristic

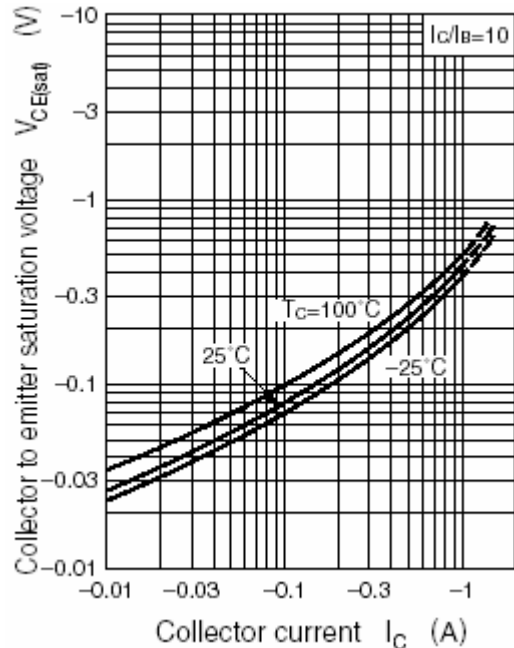


Fig.4 Collector-Emitter Saturation Voltage

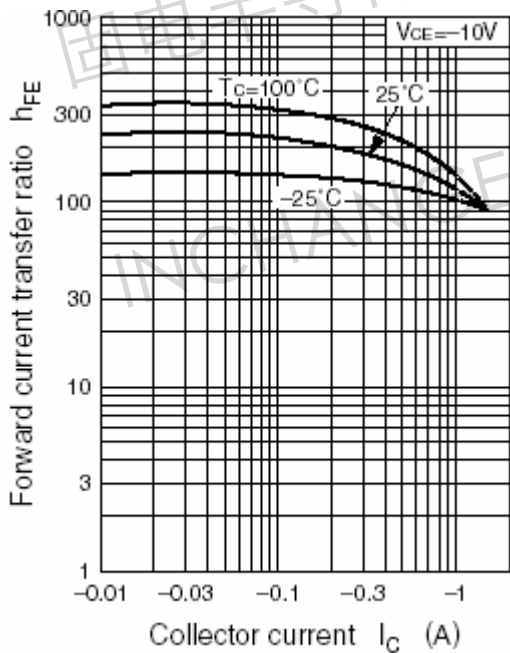


Fig.5 DC current Gain

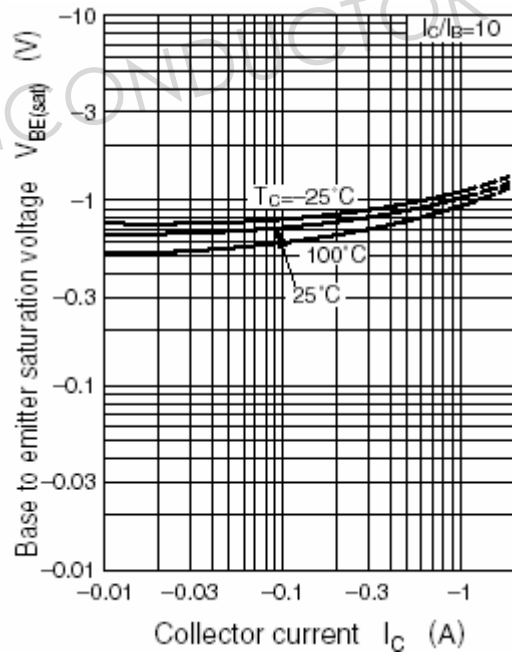


Fig.6 Base-Emitter Saturation Voltage

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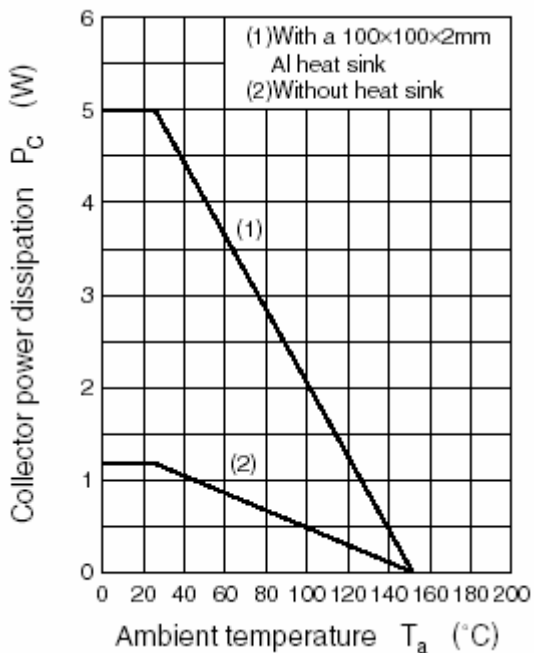


Fig.7 Power Derating

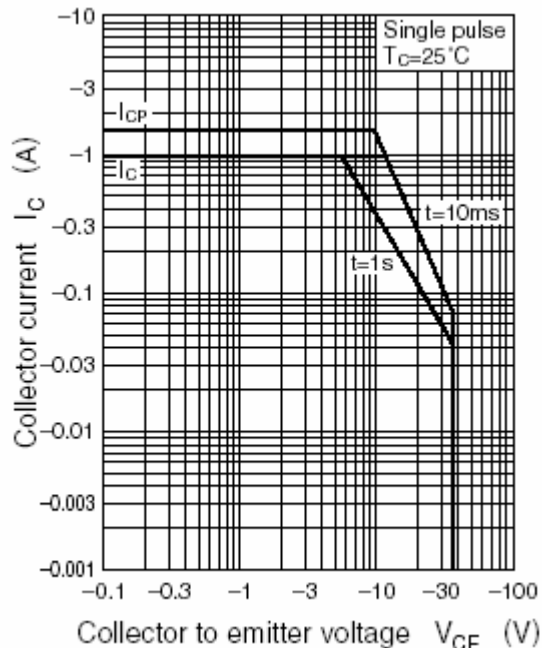


Fig.8 Safe Operating Area

固电半导体

INCHANGE SEMICONDUCTOR