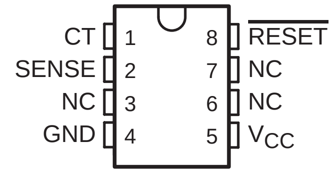
- **Adjustable Sense Voltage With Two External Resistors**
- **Adjustable Hysteresis of Sense Voltage**
- **Wide Operating Supply-Voltage Range . . . 1.8 V to 40 V**
- **Wide Operating Temperature Range . . . −40°C to 85°C**
- **Low Power Consumption (I_{CC} = 0.6 mA TYP, V_{CC} = 40 V)**
- **Minimum External Components**

P, PS, OR PW PACKAGE (TOP VIEW)



NC − No internal connection

description/ordering information

The TL7700 is a bipolar integrated circuit designed for use as a reset controller in microcomputer and microprocessor systems. The SENSE voltage can be set to any value greater than 0.5 V using two external resistors. The hysteresis value of the sense voltage also can be set by the same resistors. The device includes a precision voltage reference, fast comparator, timing generator, and output driver, so it can generate a power-on reset signal in a digital system.

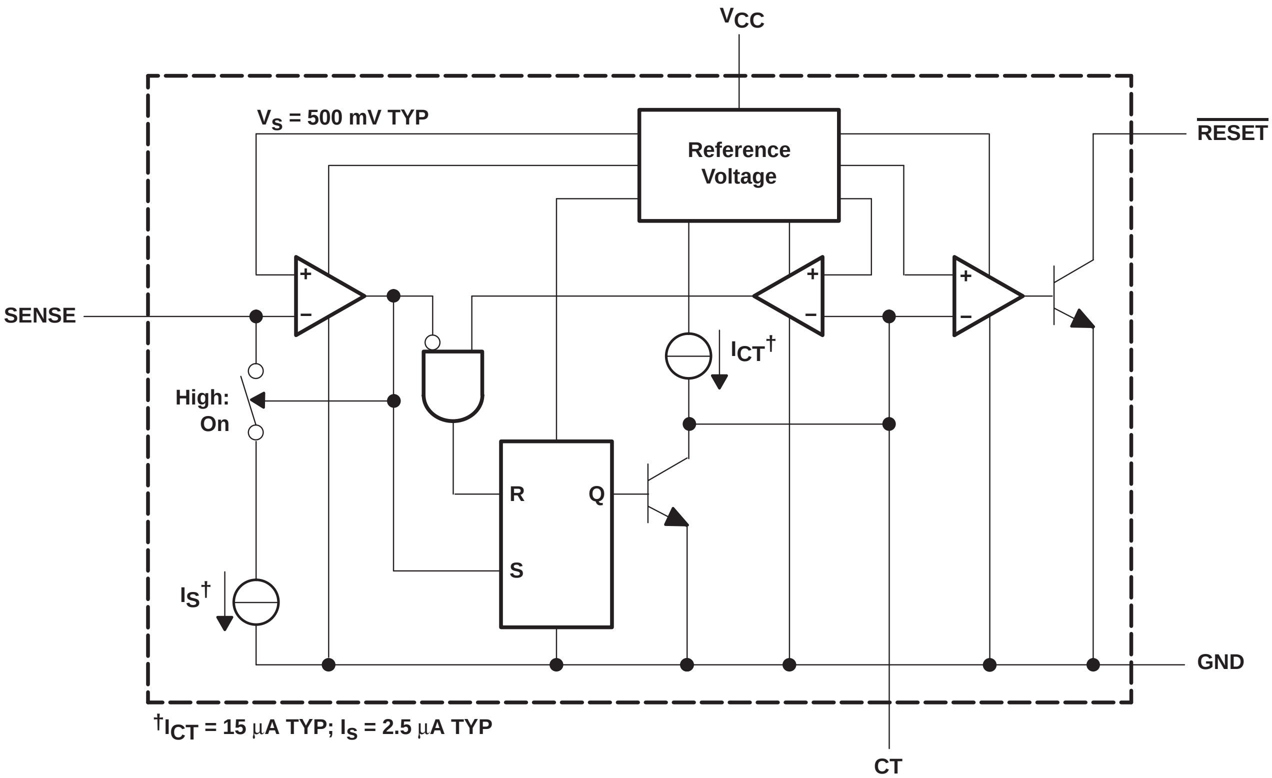
The TL7700 has an internal 1.5-V temperature-compensated voltage reference from which all function blocks are supplied. Circuit function is very stable, with supply voltage in the 1.8-V to 40-V range. Minimum supply current allows use with ac line operation, portable battery operation, and automotive applications.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
−40°C to 85°C	PDIP (P)	Tube of 50	TL7700CP	TL7700CP
	SOP (PS)	Reel of 2000	TL7700CPSR	T7700
	TSSOP (PW)	Tube of 150	TL7700CPW	T7700
		Reel of 2000	TL7700CPWR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

functional block diagram



Terminal Functions

TERMINAL NAME	NO.	DESCRIPTION
CT	1	Timing capacitor connection. This terminal sets the $\overline{\text{RESET}}$ output pulse duration (t_{po}). It is connected internally to a 15-µA constant-current source. There is a limit on the switching speed of internal elements; even if CT is set to 0, response speeds remain at approximately 5 to 10 µs. If CT is open, the device can be used as an adjustable-threshold noninverting comparator. If CT is low, the internal output-stage comparator is active, and the $\overline{\text{RESET}}$ output transistor is on. An external voltage must not be applied to this terminal due to the internal structure of the device. Therefore, drive the device using an open-collector transistor, FET, or 3-state buffer (in the low-level or high-impedance state).
GND	4	Ground. Keep this terminal as low impedance to reduce circuit noise.
NC	3, 6, 7	No internal connection
$\overline{\text{RESET}}$	8	Reset output. This terminal can be connected directly to a system that resets in the active-low state. A pullup resistor usually is required because the output is an npn open-collector transistor. An additional transistor should be connected when the active-high reset or higher output current is required.
SENSE	2	Voltage sense. This terminal has a threshold level of 500 mV. The sense voltage and hysteresis can be set at the same time when the two voltage-dividing resistors are connected. The reference voltage is temperature compensated to inhibit temperature drift in the threshold voltage within the operating temperature range.
V_{CC}	5	Power supply. This terminal is used in an operating-voltage range of 1.8 V to 40 V.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} (see Note 1) . . . . 41 V
Sense input voltage range, V_S . . . . −0.3 V to 41 V
Output voltage, V_{OH} (off state) . . . . 41 V
Output current, I_{OL} (on state) . . . . 5 mA
Package thermal impedance, θ_{JA} (see Notes 2 and 3): P package . . . . 85°C/W
PS package . . . . 95°C/W
PW package . . . . 149°C/W
Operating virtual junction temperature, T_J . . . . 150°C
Storage temperature range, T_{stg} . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values are with respect to the network ground terminal.
2. Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can impact reliability.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	1.8	40	V
I_{OL}	Low-level output current		3	mA
T_A	Operating free-air temperature	−40	85	°C

electrical characteristics, V_{CC} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_S	SENSE input voltage		495	500	505	mV
		T_A = −40°C to 85°C	490		510	
I_S	SENSE input current	V_S = 0.4 V	2	2.5	3	µA
		V_S = 0.4 V, T_A = −40°C to 85°C	1.5		3.5	
I_{CC}	Supply current	V_{CC} = 40 V, V_S = 0.6 V, No load		0.6	1	mA
V_{OL}	Low-level output voltage	I_{OL} = 1.5 mA			0.4	V
		I_{OL} = 3 mA			0.8	
I_{OH}	High-level output current	V_{OH} = 40 V, V_S = 0.6 V, T_A = −40°C to 85°C			1	µA
I_{CT}	Timing-capacitor charge current	V_S = 0.6 V	11	15	19	µA

switching characteristics, V_{CC} = 3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pi}	SENSE pulse duration	C_T = 0.01 µF	2			µs
t_{po}	Output pulse duration	C_T = 0.01 µF	0.5	1	1.5	ms
t_r	Output rise time	C_T = 0.01 µF, R_L = 2.2 kΩ, C_L = 100 pF			15	µs
t_f	Output fall time	C_T = 0.01 µF, R_L = 2.2 kΩ, C_L = 100 pF			0.5	µs
t_{pd}	Propagation delay time, SENSE to output	C_T = 0.01 µF			10	µs

PARAMETER MEASUREMENT INFORMATION

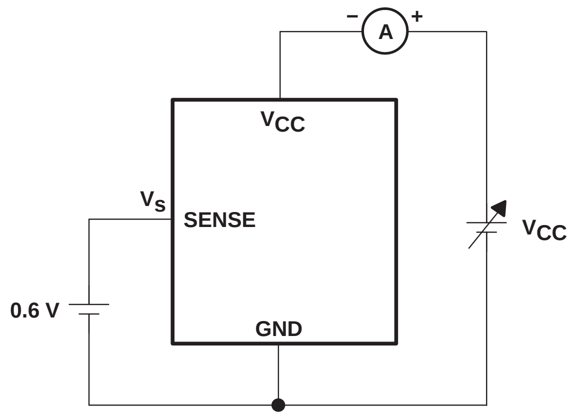


Figure 1. V_{CC} vs I_{CC} Measurement Circuit

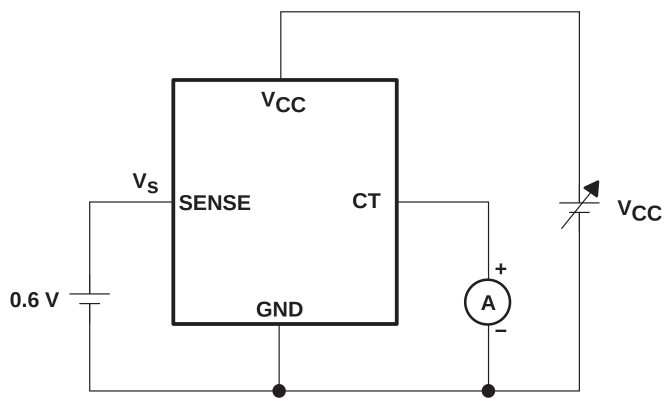


Figure 2. V_{CC} vs I_{CT}

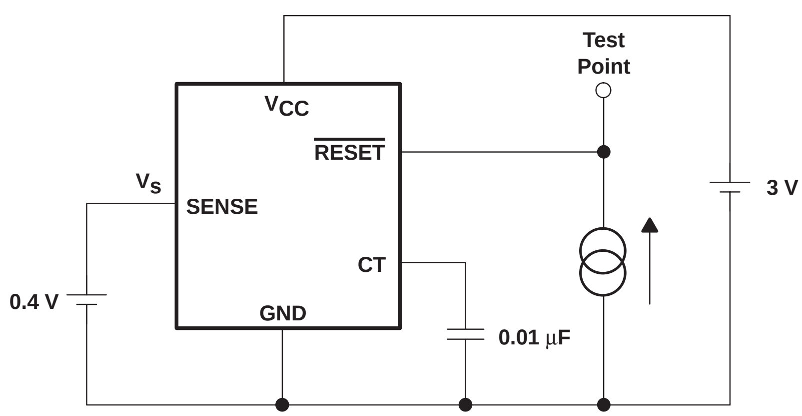


Figure 3. I_{OL} vs V_{OL}

PARAMETER MEASUREMENT INFORMATION

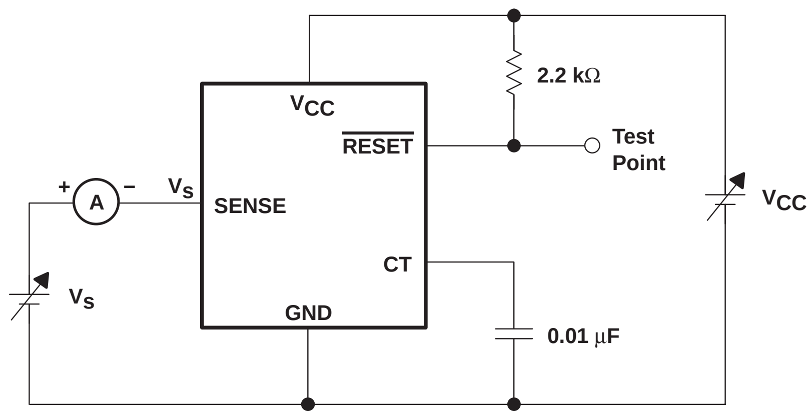


Figure 4. V_S, I_S Characteristics

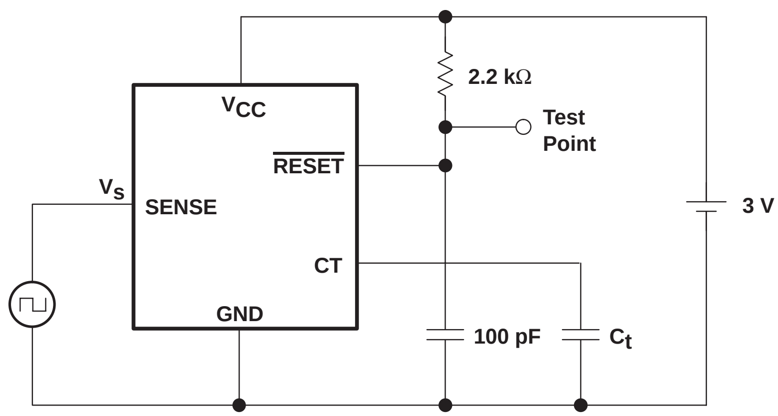


Figure 5. Switching Characteristics

TYPICAL CHARACTERISTICS†

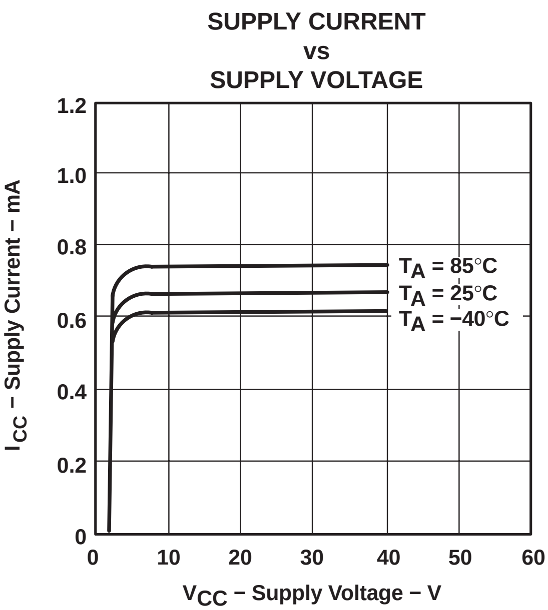


Figure 6

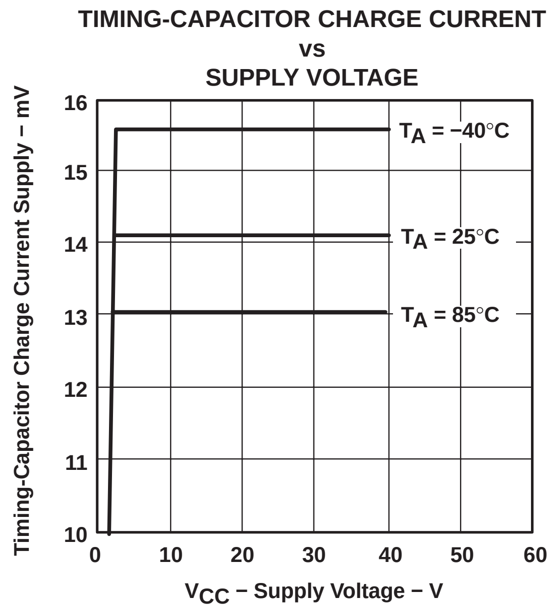


Figure 7

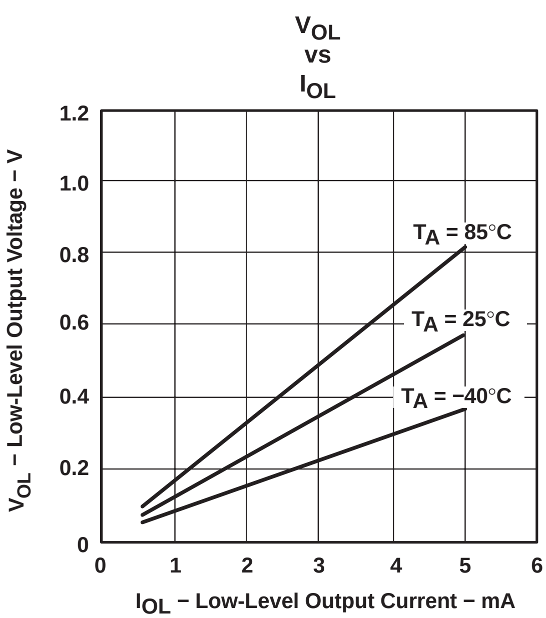


Figure 8

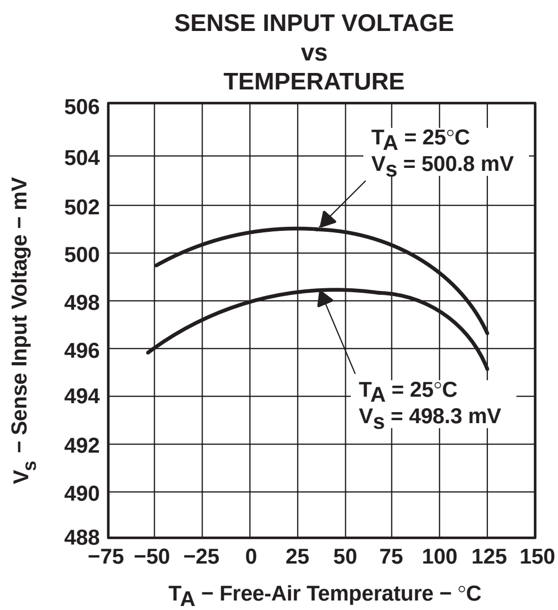


Figure 9

† Data at high and low temperatures are applicable only within the recommended operating conditions.

TYPICAL CHARACTERISTICS†

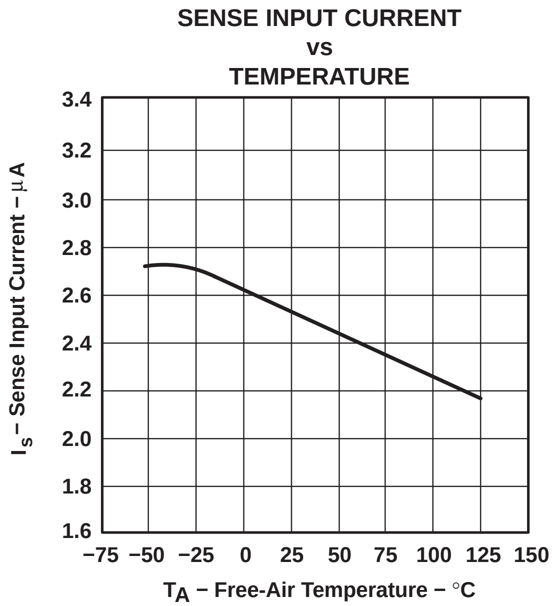


Figure 10

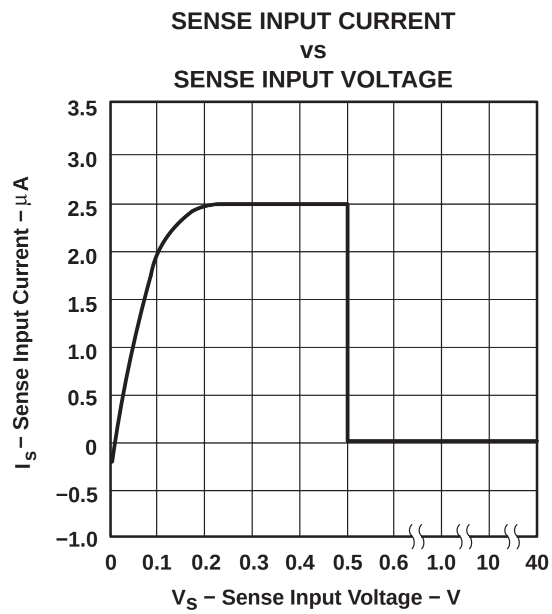


Figure 11

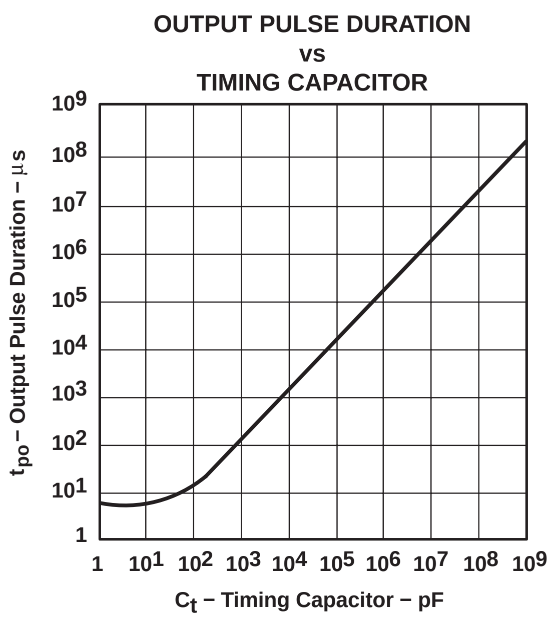


Figure 12

† Data at high and low temperatures are applicable only within the recommended operating conditions.

TYPICAL CHARACTERISTICS

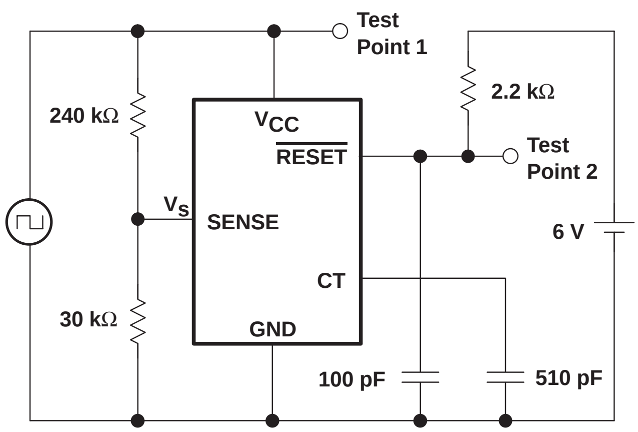


Figure 13. V_{CC} vs Output Test Circuit 1

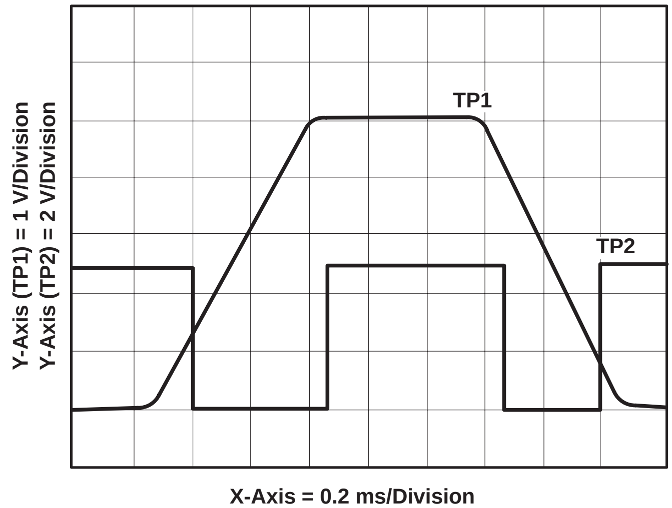


Figure 14. V_{CC} vs Output Waveform 1

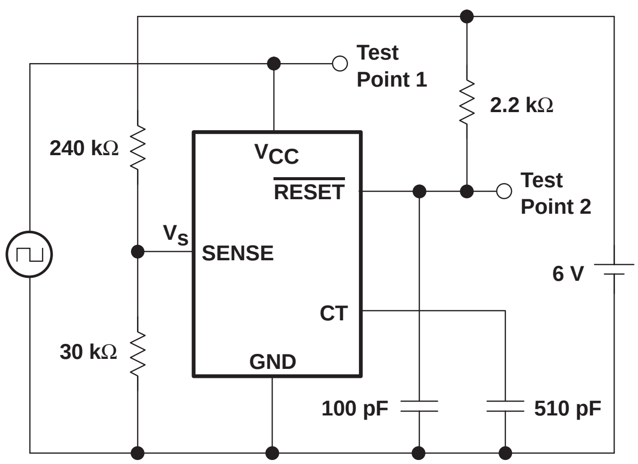


Figure 15. V_{CC} vs Output Test Circuit 2

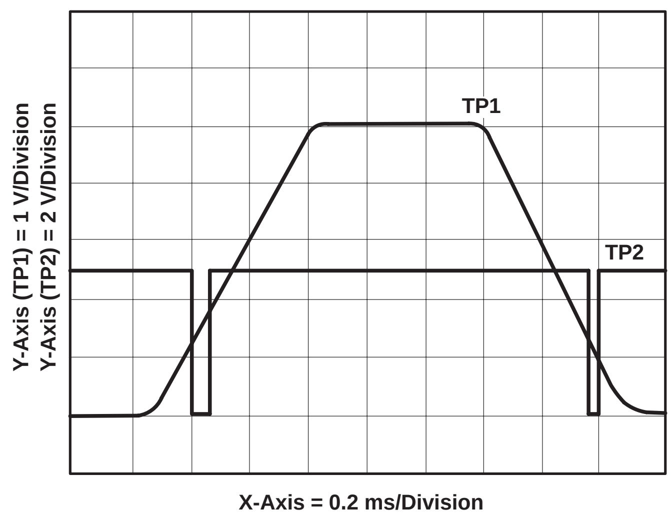


Figure 16. V_{CC} vs Output Waveform 2

TYPICAL CHARACTERISTICS

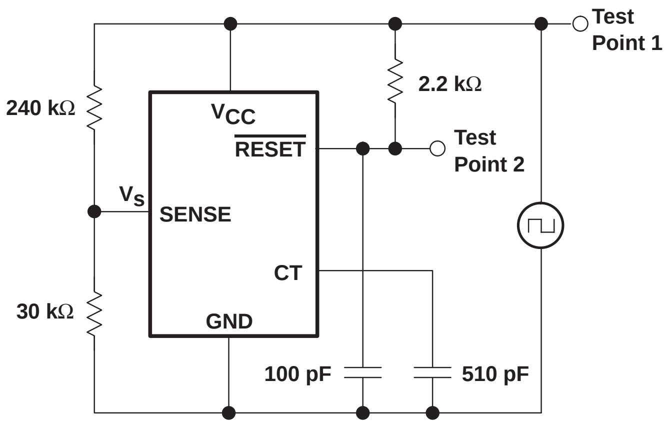


Figure 17. V_{CC} vs Output Test Circuit 3

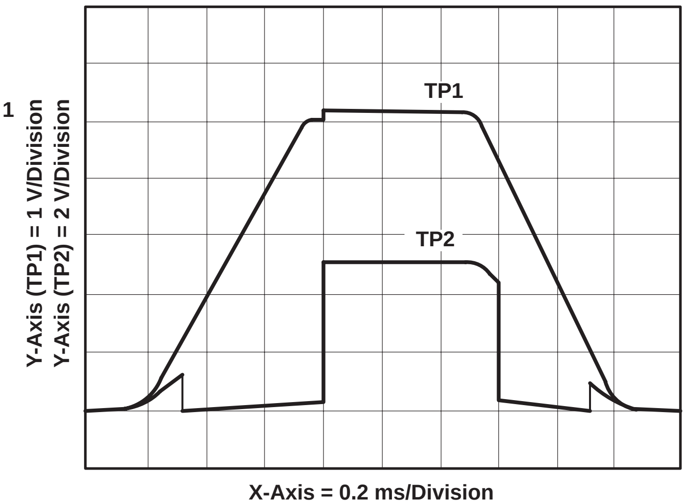


Figure 18. V_{CC} vs Output Waveform 3

detailed description

sense-voltage setting

The SENSE terminal input voltage, V_S, of the TL7700 typically is 500 mV. By using two external resistors, the circuit designer can obtain any sense voltage over 500 mV. In Figure 19, the sensing voltage, $V_{S'}$, is calculated as:

$V_{S'} = V_S \times (R1 + R2)/R2$

Where:
V_S = 500 mV, typically at T_A = 25°C

At room temperature, V_S has a variation of 500 mV ± 5 mV. In the basic circuit shown in Figure 19, variations of [±5 × (R1 + R2)/R2] mV are superimposed on V_S.

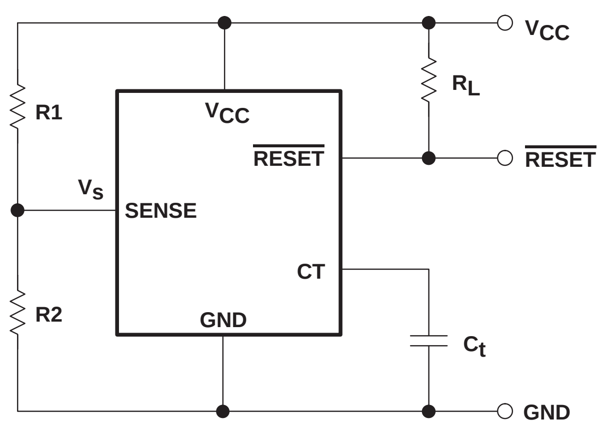


Figure 19

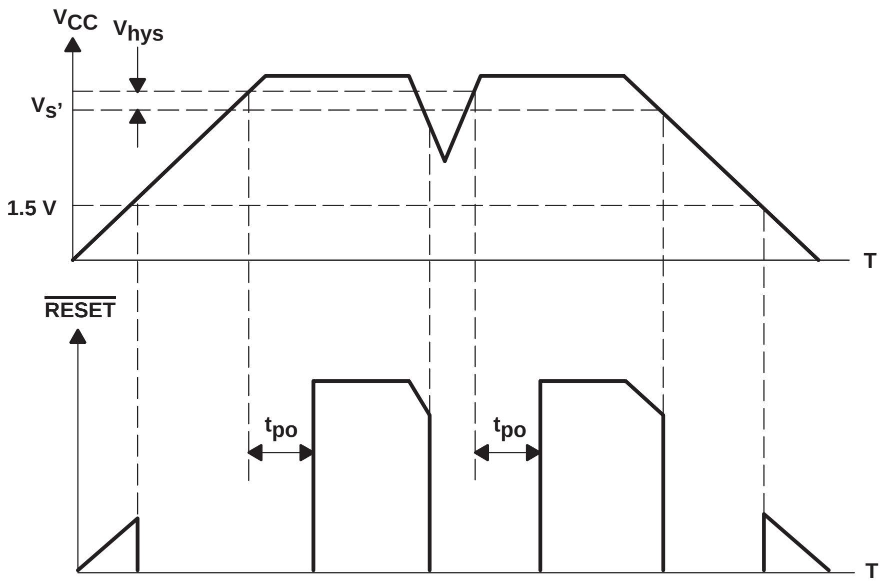
sense-voltage hysteresis setting

If the sense voltage, $V_{S'}$, does not have hysteresis in it, and the voltage on the sensing line contains ripples, the resetting of TL7700 will be unstable. Hysteresis is added to the sense voltage to prevent such problems. As shown in Figure 20, the hysteresis, V_{hys}, is added, and the value is determined as:

$V_{hys} = I_S \times R1$

Where:
I_S = 2.5 μA, typically at T_A = 25°C

At room temperature, I_S has variations of 2.5 μA ± 0.5 μA. Therefore, in the circuit shown in Figure 19, V_{hys} has variations of (±0.5 × R1) μV. In circuit design, it is necessary to consider the voltage-dividing resistor tolerance and temperature coefficient in addition to variations in V_S and V_{hys}.



NOTE A: The sense voltage, $V_{S'}$, is different from the SENSE terminal input voltage, V_S. V_S normally is 500 mV for triggering.

Figure 20. V_{CC}-RESET Timing Chart

output pulse-duration setting

Constant-current charging starts on the timing capacitor when the sensing-line voltage reaches the TL7700 sense voltage. When the capacitor voltage exceeds the threshold level of the output drive comparator, $\overline{RESET}$ changes from a low to a high level. The output pulse duration is the time between the point when the sense-pin voltage exceeds the threshold level and the point when the $\overline{RESET}$ output changes from a low level to a high level. When the TL7700 is used for system power-on reset, the output pulse duration, t_{po}, must be set longer than the power rise time. The value of t_{po} is:

$t_{po} = C_t \times 10^5$ seconds

Where:
C_t is the timing capacitor in farads

There is a limit on the device response speed. Even if C_t = 0, t_{po} is not 0, but approximately 5 μs to 10 μs. Therefore, when the TL7700 is used as a comparator with hysteresis, without connecting C_t, switching speeds (t_r/t_f, t_{po}/t_{pd}, etc.) must be considered.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
TL7700CP	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL7700CPE4	ACTIVE	PDIP	P	8	50	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
TL7700CPSR	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL7700CPSRG4	ACTIVE	SO	PS	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL7700CPW	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL7700CPWE4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL7700CPWG4	ACTIVE	TSSOP	PW	8	150	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL7700CPWR	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL7700CPWRE4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
TL7700CPWRG4	ACTIVE	TSSOP	PW	8	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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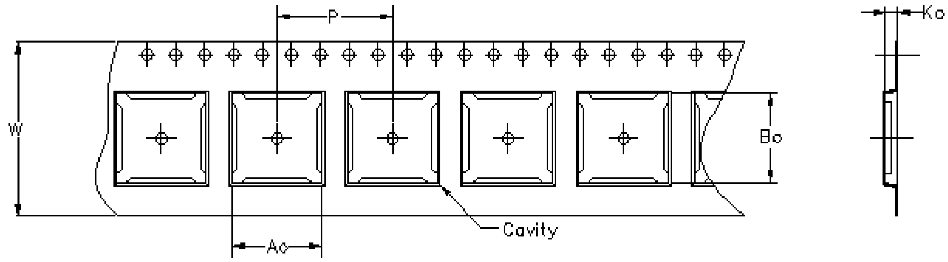
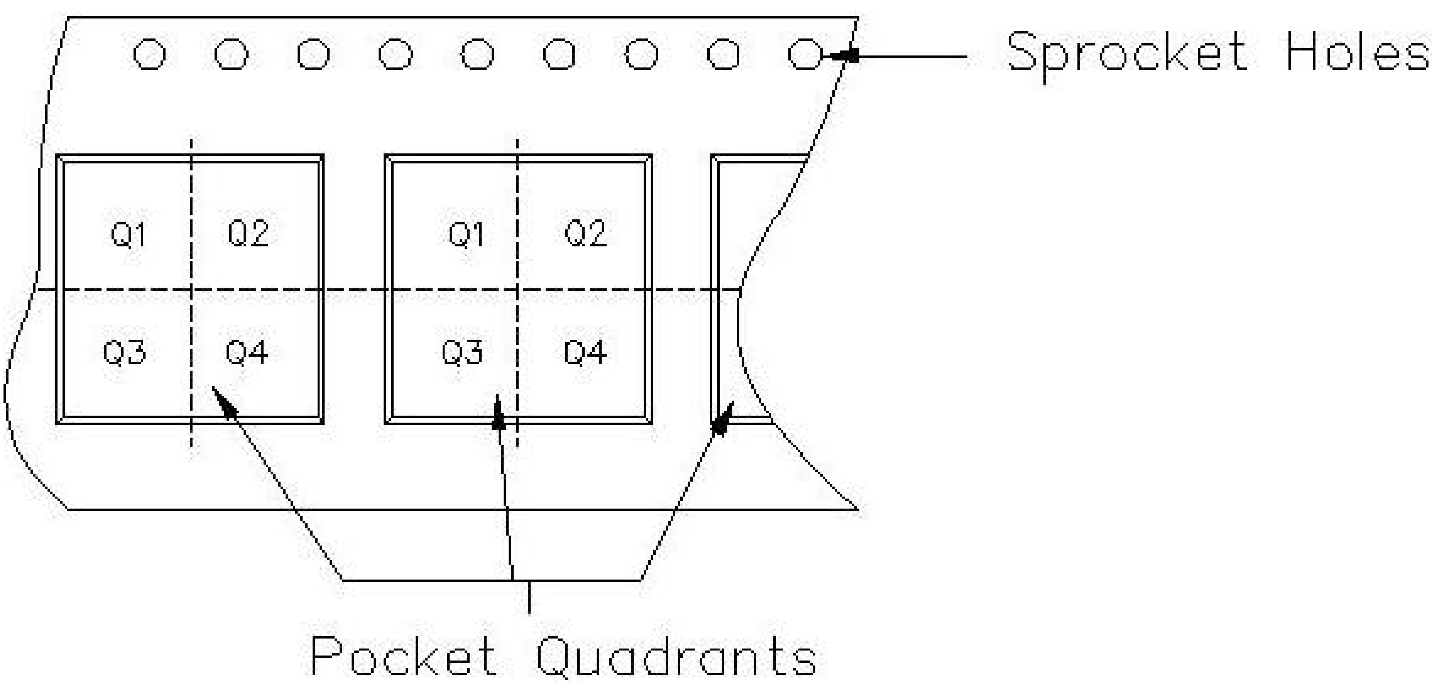
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE MATERIALS INFORMATION



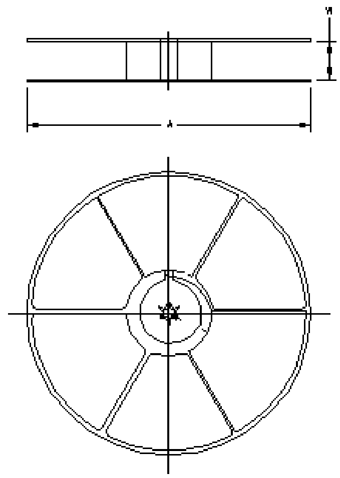
Carrier tape design is defined largely by the component lentgh, width, and thickness.

Ao = Dimension designed to accommodate the component width.
Bo = Dimension designed to accommodate the component length.
Ko = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



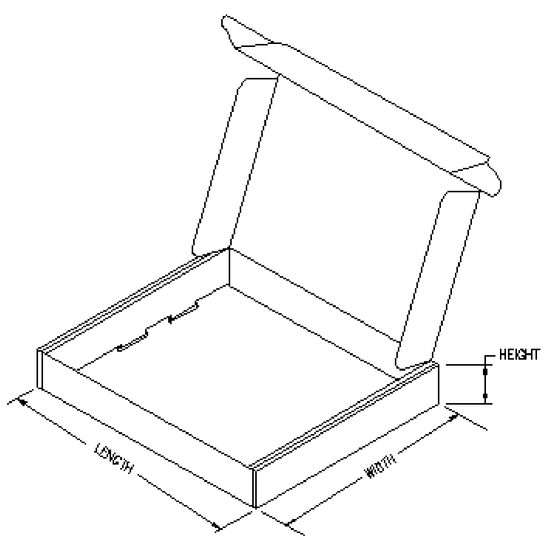
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL7700CPSR	PS	8	MLA	330	16	8.2	6.6	2.5	12	16	Q1
TL7700CPWR	PW	8	MLA	330	12	7.0	3.6	1.6	8	12	Q1

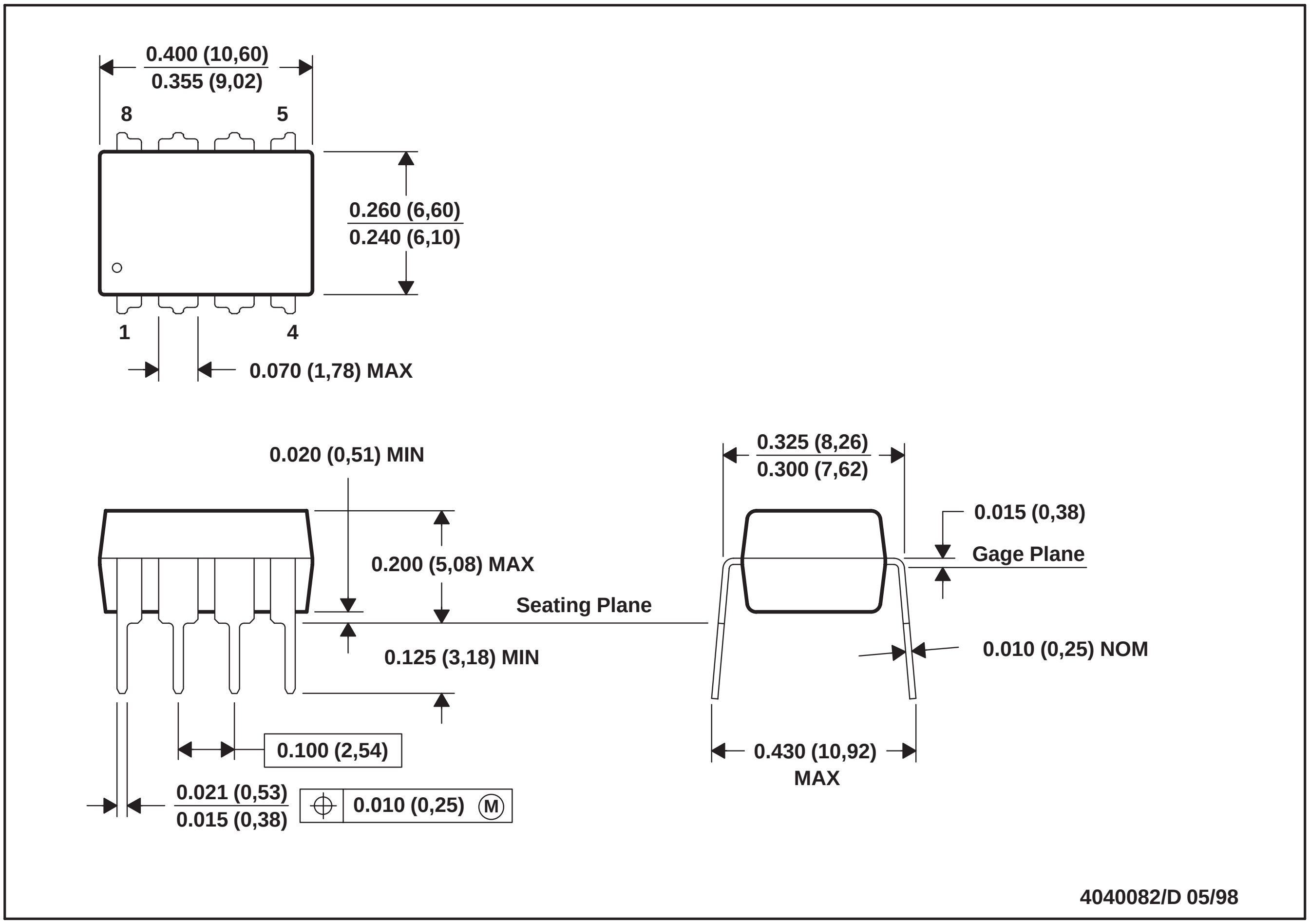


TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
TL7700CPSR	PS	8	MLA	342.9	336.6	28.58
TL7700CPWR	PW	8	MLA	338.1	340.5	20.64

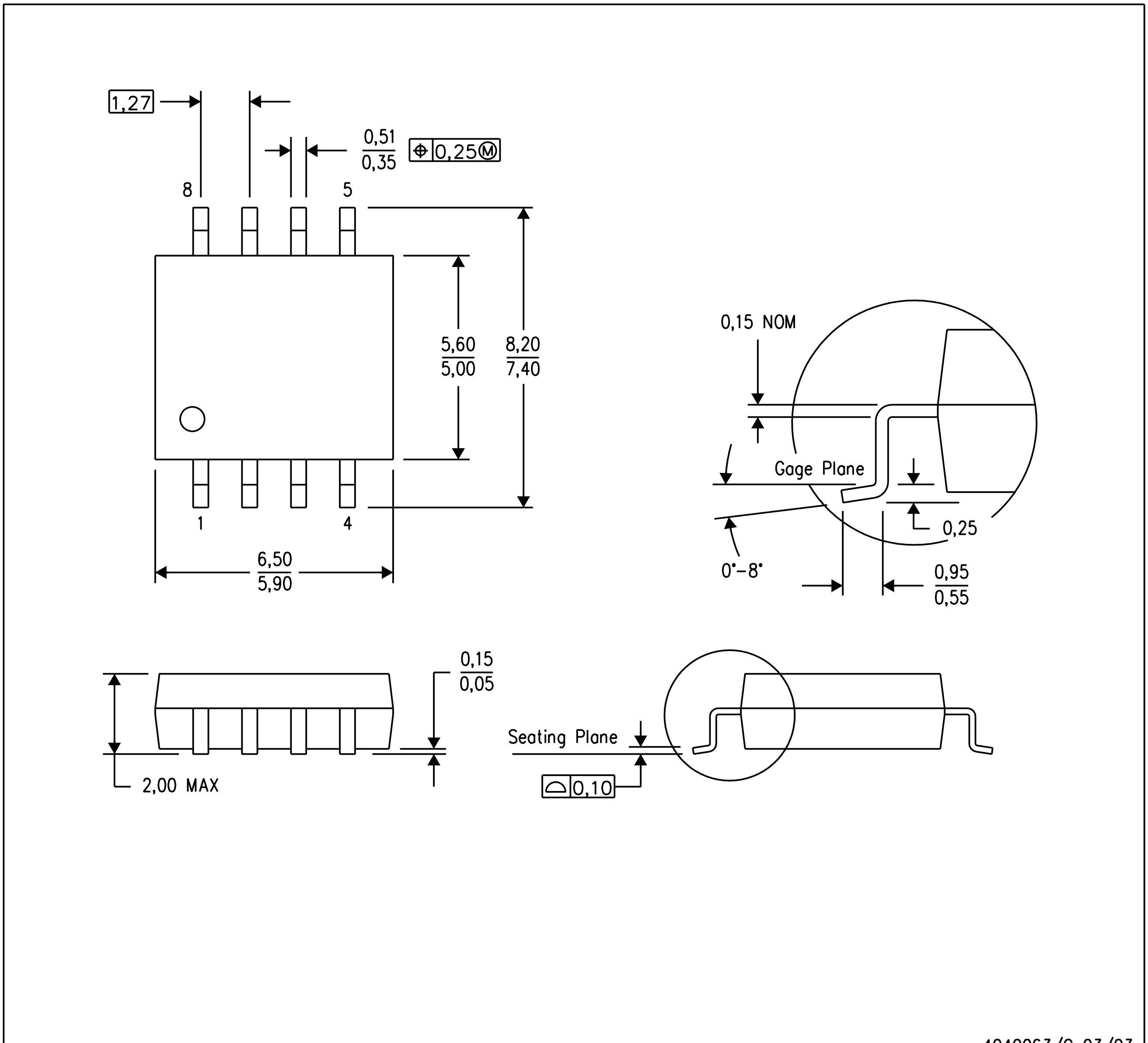


P (R-PDIP-T8) **PLASTIC DUAL-IN-LINE**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001

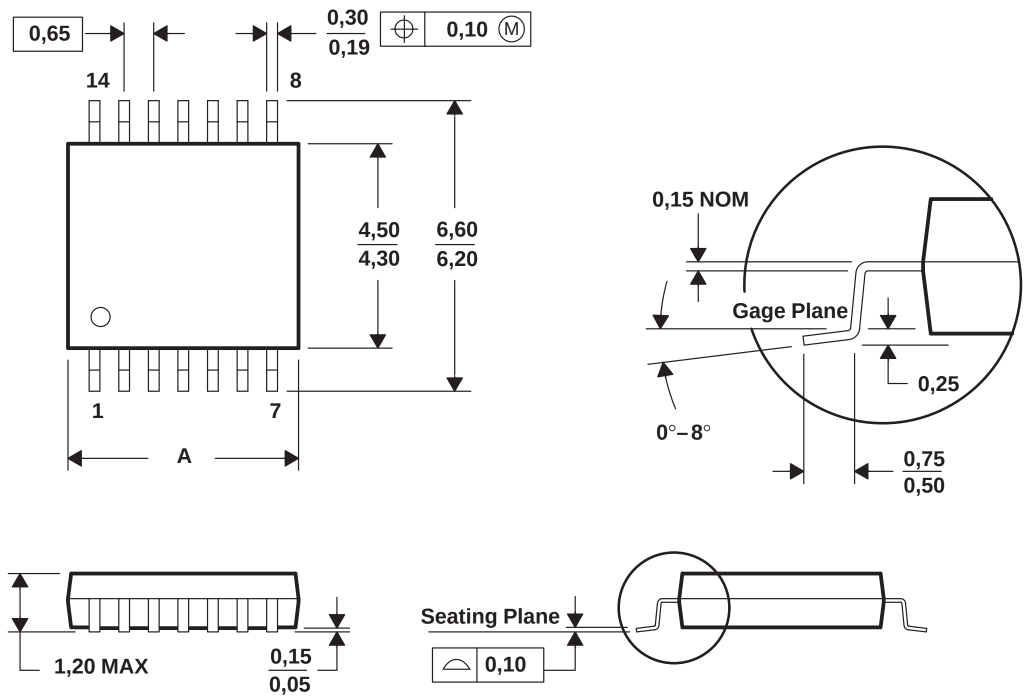
PS (R-PDSO-G8) **PLASTIC SMALL-OUTLINE PACKAGE**



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



PINS ** / DIM	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153