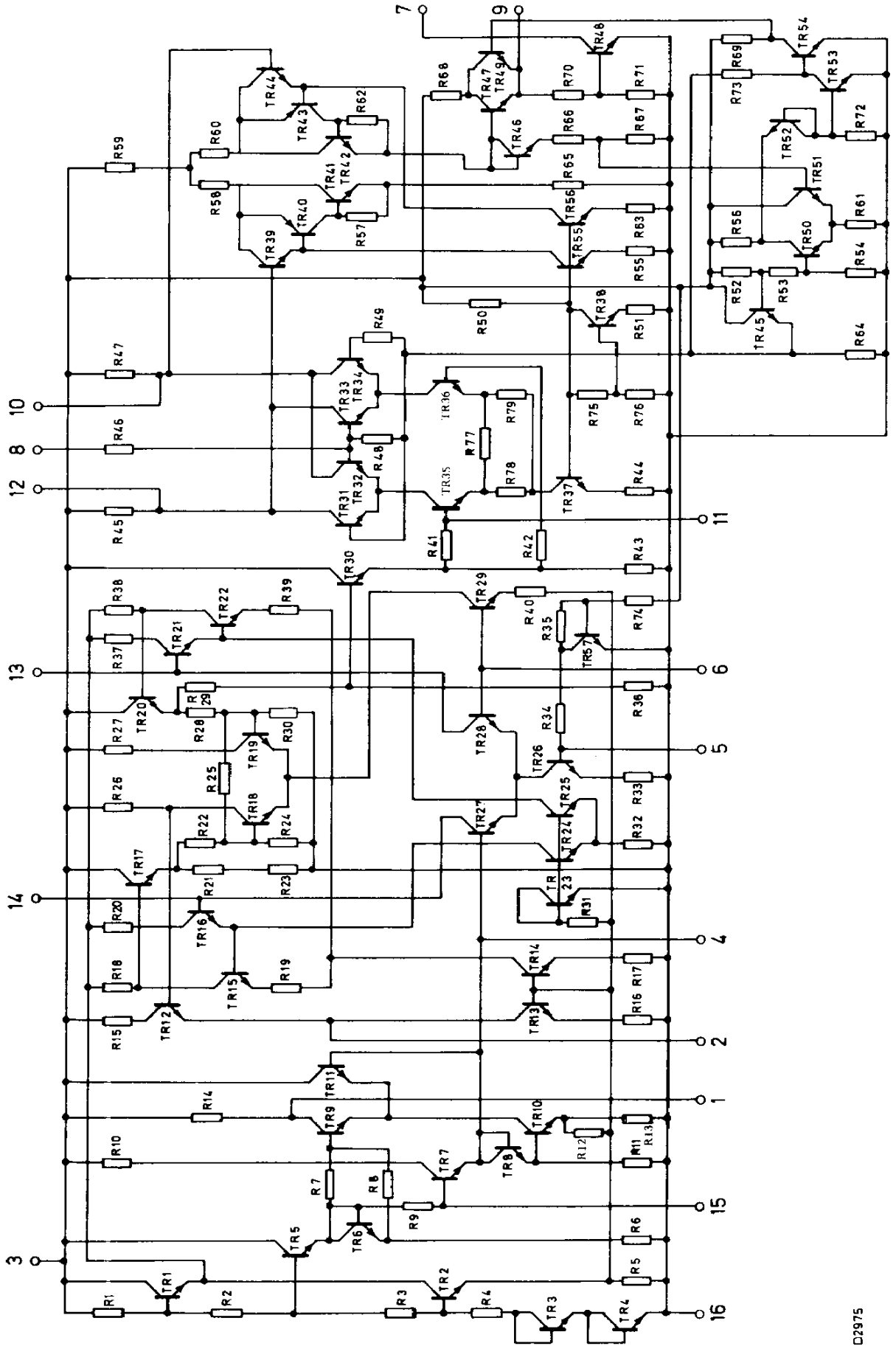


CIRCUIT DIAGRAM



48

RATINGS Limiting values in accordance with the Absolute Maximum System (IEC 134)

Voltage

Supply voltage V₃₋₁₆ max. 13.2 V

Power dissipation

Total power dissipation at T_{amb} = 50 °C P_{tot} max. 680 mW

Temperatures

Storage temperature T_{stg} -55 to +125 °C

Operating ambient temperature T_{amb} -20 to +60 °C

CHARACTERISTICS at V₃₋₁₆ = 12 V; T_{amb} = 25 °C; V_{5-16 M} = 0.7 V (burst signal input); V_{8-16(p-p)} = 2.5 V (P. A. L. square wave input) Measured in circuit shown on page 4.

Output signals

R-Y reference signal output
peak-to-peak value V_{4-16(p-p)} typ. 1.5 V

Colour killer output: colour on V₇₋₁₆ typ. 12 V
colour off V₇₋₁₆ < 250 mV

A.C.C. output signal range

at correct phase of P. A. L. switch V₉₋₁₆ +4 to +0.2 V

at incorrect phase of P. A. L. switch V₉₋₁₆ +4 to +11 V

Oscillator section (amplifier)

Input resistance R₁₅₋₁₆ typ. 3.5 kΩ

Input capacitance C₁₅₋₁₆ typ. 5 pF

Voltage gain G₁₅₋₁ typ. 4.7

Reactance control section

Voltage gain with pins 13 and 14 interconnected G₁₅₋₂ typ. 1.3

Rate of change of gain G₁₅₋₂ with phase difference
between burst and reference signal $\frac{\Delta G_{15-2}}{\Delta \varphi_{5-4}}$ typ. 5 $\frac{1}{\text{rad}}$

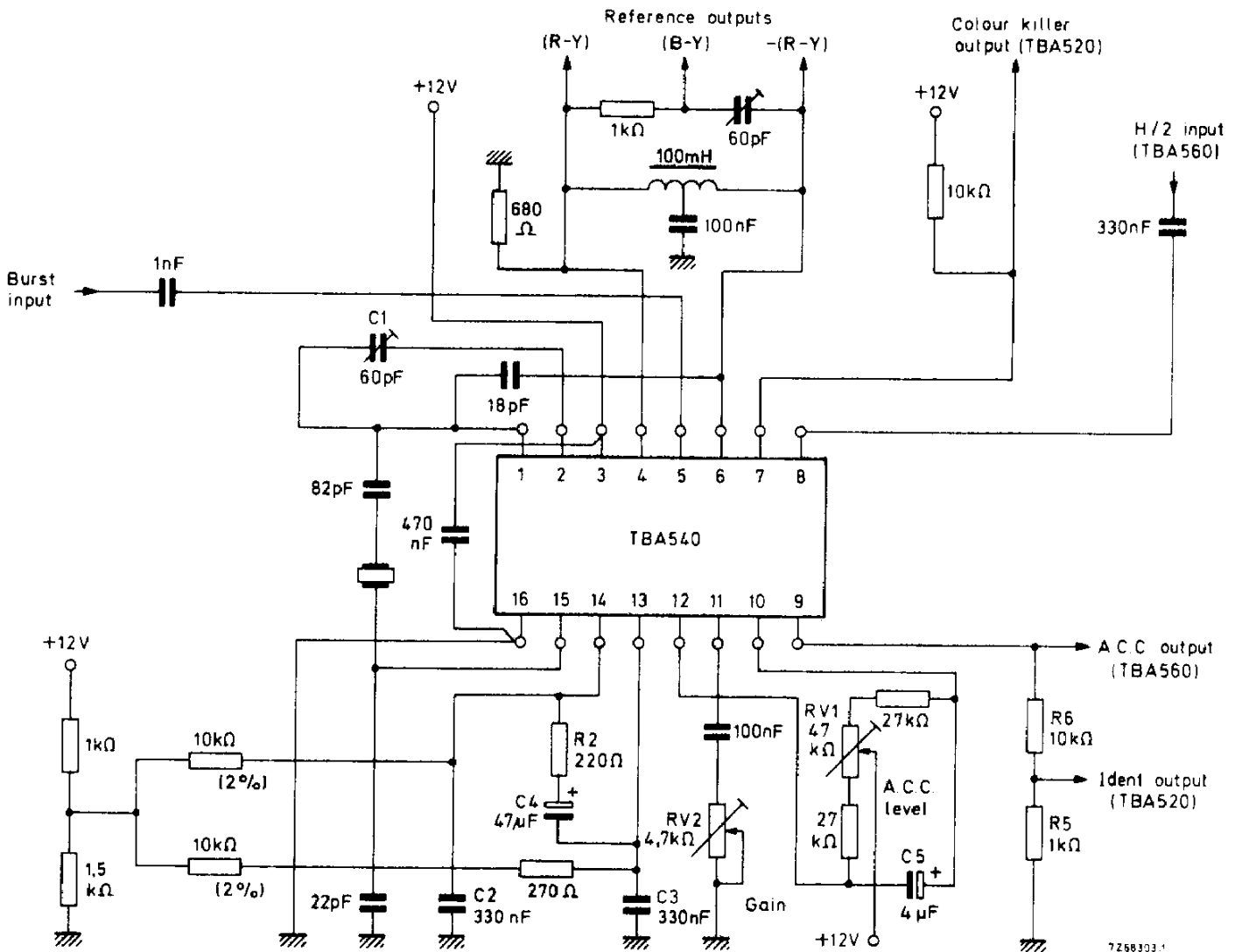
Supply current consumption I₃ typ. 33 mA

TBA540 TBA540Q

PINNING

- | | |
|---------------------------------------|--|
| 1. Oscillator feedback output | 9. A.C.C. output |
| 2. Reactance control stage feedback | 10. A.C.C. level setting (see also pin 12) |
| 3. Supply voltage (12 V) | 11. A.C.C. gain setting |
| 4. Reference waveform output | 12. A.C.C. level setting (see also pin 10) |
| 5. Burst waveform input | 13.) D.C. control points for |
| 6. Reference waveform input | 14.) oscillator phase control loop |
| 7. Colour killer output | 15. Oscillator feedback input |
| 8. P.A.L. flip-flop square wave input | 16. Earth (negative supply) |

APPLICATION INFORMATION



APPLICATION INFORMATION (continued)

The function is quoted against the corresponding pin number

1. Oscillator feedback output

The crystal receives its energy from this pin. The input impedance is approximately $2\text{ k}\Omega$ in parallel with 5 pF .

2. Reactance control stage feedback

This pin is fed internally with a sinewave derived from the reference input (pin 6) and controlled in amplitude by the internal reactance control circuit. The phase of the feedback from pin 2 to the crystal via C1 is such that the value of C1 is effectively increased. Pin 2 is held internally at a very low impedance therefore the tuning of the crystal is controlled automatically by the amplitude of the feedback waveform and its influence on the effective value of C1.

3. Positive 12 V supply

The maximum voltage must not exceed 13.2 V .

4. Reference waveform output

This pin is driven internally by the regenerated subcarrier waveform in R-Y phase. An output amplitude of nominally 1.5 V peak-to-peak is produced at low impedance. No d.c. load to earth is required. A d.c. connection between pins 4 and 6 is, however, necessary via the bifilar coupling inductor. The function of this inductor is to produce, on pin 6, a signal of equal amplitude and opposite phase $(-(R-Y))$ to that on pin 4. A centre tap on the inductor, connected to earth via a d.c. blocking capacitor, is therefore necessary.

5. Burst waveform input

A burst waveform amplitude of 1 V peak-to-peak is required to be a.c. -coupled to this pin. The amplitude of the burst will normally be controlled by the adjustment and operation of the a.c.c. circuit. The input impedance at this pin is approximately $1\text{ k}\Omega$ and a threshold level of 0.7 V must be exceeded before the burst signal becomes effective. A d.c. bias of 400 mV is internally derived for pin 5. The absolute level of the tip of the burst at pin 5 will normally reach 1.25 V (1.5 V peak-to-peak burst amplitude). Under abnormal conditions the burst amplitude should not be allowed to exceed 3 V peak-to-peak and a limiting condition will be reached in the i.c. which inhibits the performance of the phase lock loop.

APPLICATION INFORMATION (continued)

6. Reference waveform input

This pin requires a reference waveform in the -(R-Y) phase, derived from pin 4 via a bifilar transformer (see pin 4), to drive the internal balanced reactance control stage. A d.c. connection between pins 4 and 6 must be made via the transformer.

7. Colour killer output

This pin is driven from the collector of an internal switching transistor and requires an external load resistor (typical 10 k Ω) connected to +12 V. The unkill- ed and killed voltages on this pin are then +12 V and < 250 mV respectively. (The voltage on pin 9 at which switching of the colour killer output on pin 7 occurs is nominally +2.5 V

8. P.A.L. flip-flop square wave input

A 2.5 V peak-to-peak square wave derived from the P.A.L. flip-flop (in the TBA520 demodulator i.c.) is required at this pin, a.c.-coupled via a capacitor. The input impedance is about 3.3 k Ω .

9. A.C.C. output

An emitter follower provides a low impedance output potential which is negative-going with a rising burst input amplitude. With zero input signal the d.c. potential produced at pin 9 is set to be +4 V (RV1). The appearance of a burst signal on pin 5 will cause the potential on pin 9 to go in a negative direction in the event that the P.A.L. flip-flop is identified to be in the correct phase. The range of potential over which full a.c.c. control is exercised at pin 9 is determined by the control characteristics of the a.c.c. amplifier i.e. for the TBA560 from 1 V to 0.2 V. The potential at pin 9 will fall to a value within this range as the burst input signal is stabilised at 1.5 V peak-to-peak. The latter condition is achieved by correct adjustment of RV2. If, however, the P.A.L. flip-flop phase is wrong the potential on pin 9 will move positively. The potential divider R5, R6 will then operate a P.A.L. switch cut-off function in the TBA520 demodulator i.c. The switching of the colour killer output at pin 7 is designed to occur as the potential on pin 9 moves past +2.5 V.

10. A.C.C. level setting

The network connected between pins 10 and 12 balances the a.c.c. circuit and RV1 is adjusted to give +4 V on pin 9 with no burst input signal to pin 5. C5 provides filtering.

11. A.C.C. gain control

RV2 is adjusted to give the correct amplitude of burst signal on pin 5 (1.5 V peak-to-peak) under a.c.c. control;

12. See pin 10.

13. See pin 14.

APPLICATION INFORMATION (continued)14. D.C. control points in reference control loop

Pins 13 and 14 are connected to opposite sides of a differential amplifier circuit and are brought out for the purposes d. c. balancing of the reactance stage and the connection of the bandwidth-determining filter network. The conventional double time constant filter networks are R₂, C₂, R₃, C₃ and R₄, C₄. The d. c. potentials on these pins are nominally +7,2 V.

15. Oscillator feedback input

The input impedance at this pin is nominally 3.5 k Ω in parallel with 5 pF. No d. c. connection is required on this pin. The voltage in the i. c. between pin 15 and pin 1 is nominally 4.7 times.

16. Negative supply (earth)PERFORMANCE AND COMMENTSInitial adjustment

- (a) Remove burst signal.
- (b) Short-circuit pins 13-14. Adjust oscillator to correct frequency by C1. Remove short circuit.
- (c) Set the a. c. c. level adjustment RV1, to give +4 V on pin 9.
- (d) Apply burst signal.
- (e) Adjust a. c. c. gain, RV 2, to give a burst amplitude of 1.5 V peak-to-peak on pin 5.

Phase lock loop performance (with crystal type 4322 152 0110)

- (a) Phase difference between reference and burst signals for ± 400 Hz deviation of crystal frequency, $\pm 10^\circ$.
- (b) Typical holding range, ± 600 Hz.
- (c) Typical pull-in range, ± 300 Hz.
- (d) Temperature coefficient of oscillator frequency, i. c. only, 2 Hz/ $^\circ$ C.