

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT643**

Octal bus transceiver; 3-state;  
true/inverting

Product specification  
File under Integrated Circuits, IC06

December 1990

# Octal bus transceiver; 3-state; true/inverting

## 74HC/HCT643

### FEATURES

- Octal bidirectional bus interface
- True and inverting 3-state outputs
- Output capability: bus driver
- $I_{CC}$  category: MSI

### GENERAL DESCRIPTION

The 74HC/HCT643 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT643 are octal transceivers featuring true and inverting 3-state bus compatible outputs in both send and receive directions.

The "643" features an output enable ( $\overline{OE}$ ) input for easy cascading and a send/receive (DIR) for direction control.  $\overline{OE}$  controls the outputs so that the buses are effectively isolated.

### QUICK REFERENCE DATA

GND = 0 V;  $T_{amb} = 25\text{ }^{\circ}\text{C}$ ;  $t_r = t_f = 6\text{ ns}$

| SYMBOL            | PARAMETER  | CONDITIONS                                   | TYPICAL |         | UNIT     |
|-------------------|--|--|---------|---------|----------|
|                   |  |  | HC      | HCT     |          |
| $t_{PHL}/t_{PLH}$ | propagation delay<br>A <sub>n</sub> to B <sub>n</sub> ; inverting<br>B <sub>n</sub> to A <sub>n</sub> ; true | $C_L = 15\text{ pF}$ ; $V_{CC} = 5\text{ V}$ | 7<br>8  | 8<br>11 | ns<br>ns |
| $C_I$             | input capacitance  |  | 3.5     | 3.5     | pF       |
| $C_{I/O}$         | input/output capacitance   |  | 10      | 10      | pF       |
| $C_{PD}$          | power dissipation capacitance per transceiver  | notes 1 and 2                                | 42      | 44      | pF       |

### Notes

1.  $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu\text{W}$ ):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

$f_i$  = input frequency in MHz

$f_o$  = output frequency in MHz

$\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs

$C_L$  = output load capacitance in pF

$V_{CC}$  = supply voltage in V

2. For HC the condition is  $V_I = \text{GND to } V_{CC}$   
For HCT the condition is  $V_I = \text{GND to } V_{CC} - 1.5\text{ V}$

### ORDERING INFORMATION

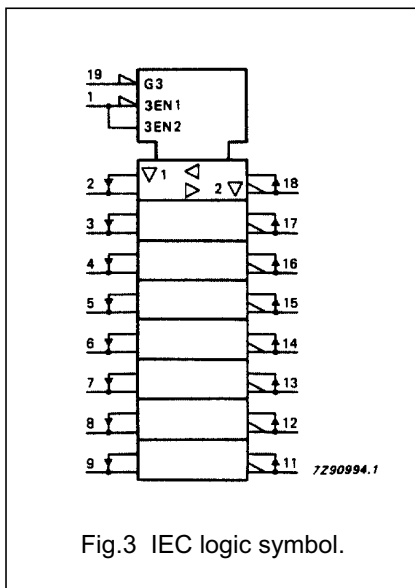
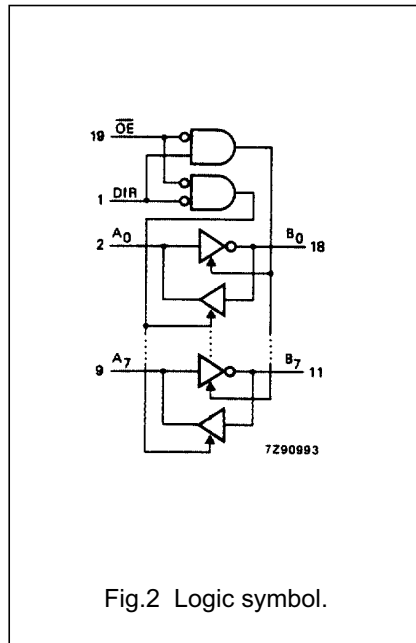
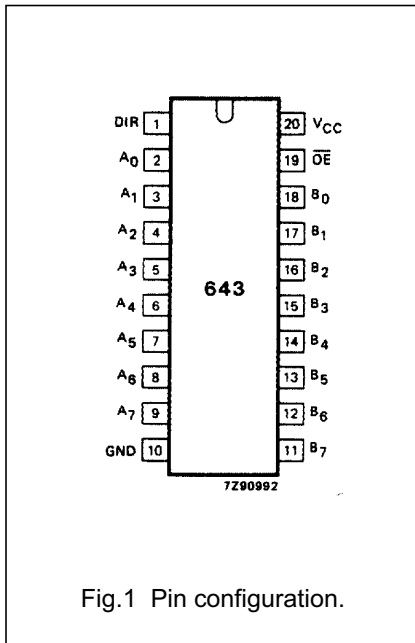
See "74HC/HCT/HCU/HCMOS Logic Package Information".

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PIN DESCRIPTION

| PIN NO.                        | SYMBOL                           | NAME AND FUNCTION                |
|--------------------------------|----------------------------------|----------------------------------|
| 1                              | DIR                              | direction control                |
| 2, 3, 4, 5, 6, 7, 8, 9         | A <sub>0</sub> to A <sub>7</sub> | data inputs/outputs              |
| 10                             | GND                              | ground (0 V)                     |
| 18, 17, 16, 15, 14, 13, 12, 11 | B <sub>0</sub> to B <sub>7</sub> | data inputs/outputs              |
| 19                             | $\overline{OE}$                  | output enable input (active LOW) |
| 20                             | V <sub>CC</sub>                  | positive supply voltage          |

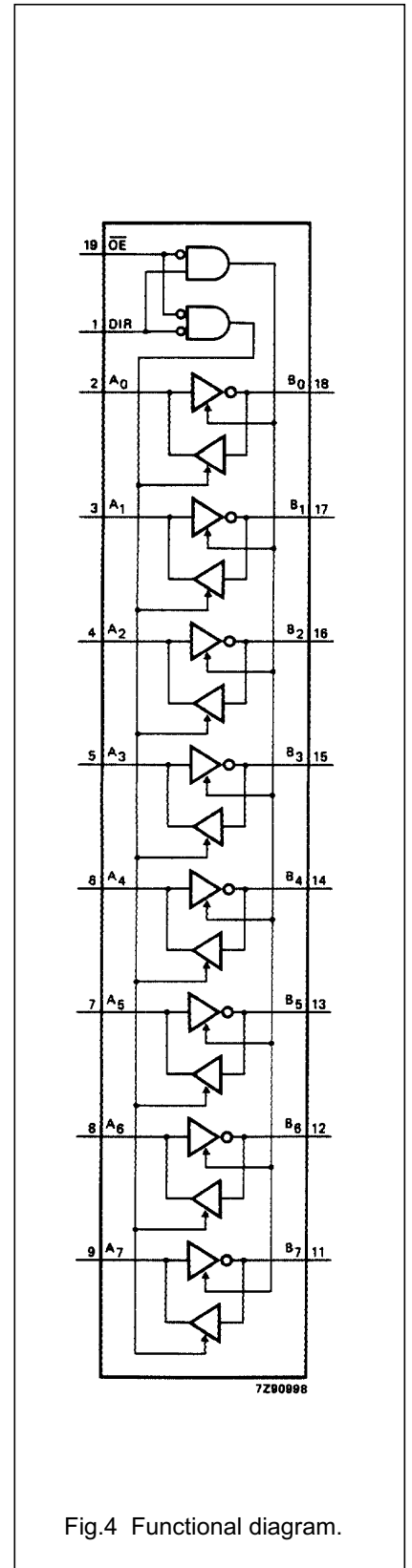


FUNCTION TABLE

| INPUTS          |     | INPUTS/OUTPUTS |                    |
|-----------------|-----|----------------|--------------------|
| $\overline{OE}$ | DIR | A <sub>n</sub> | B <sub>n</sub>     |
| L               | L   | A = B          | inputs             |
| L               | H   | inputs         | B = $\overline{A}$ |
| H               | X   | Z              | Z                  |

Notes

- H = HIGH voltage level  
L = LOW voltage level  
X = don't care  
Z = high impedance OFF-state



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**DC CHARACTERISTICS FOR 74HC**For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

 $I_{CC}$  category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

| SYMBOL            | PARAMETER   | $T_{amb}$ (°C) |                |                 |            |                 |             | UNIT            | TEST CONDITIONS |                   |                 |
|-------------------|---|----------------|----------------|-----------------|------------|-----------------|-------------|-----------------|-----------------|-------------------|-----------------|
|                   |   | 74HC           |                |                 |            |                 |             |                 | $V_{CC}$<br>(V) | WAVEFORMS         |                 |
|                   |   | +25            |                |                 | -40 to +85 |                 | -40 to +125 |                 |                 |                   |                 |
|                   |   | min.           | typ.           | max.            | min.       | max.            | min.        |                 |                 |                   | max.            |
| $t_{PHL}/t_{PLH}$ | propagation delay<br>$A_n$ to $B_n$ ;<br>inverting  |                | 25<br>9<br>7   | 90<br>18<br>15  |            | 115<br>23<br>20 |             | 135<br>27<br>23 | ns              | 2.0<br>4.5<br>6.0 | Fig.5           |
| $t_{PHL}/t_{PLH}$ | propagation delay<br>$B_n$ to $A_n$ ;<br>non-inverting (true)                                     |                | 28<br>10<br>8  | 90<br>18<br>15  |            | 115<br>23<br>20 |             | 135<br>27<br>23 | ns              | 2.0<br>4.5<br>6.0 | Fig.6           |
| $t_{PZH}/t_{PZL}$ | 3-state output enable time<br>$\overline{OE}$ , DIR to $A_n$ ;<br>$\overline{OE}$ , DIR to $B_n$  |                | 39<br>14<br>11 | 150<br>30<br>26 |            | 190<br>38<br>33 |             | 225<br>45<br>38 | ns              | 2.0<br>4.5<br>6.0 | Fig.7           |
| $t_{PHZ}/t_{PLZ}$ | 3-state output disable time<br>$\overline{OE}$ , DIR to $A_n$ ;<br>$\overline{OE}$ , DIR to $B_n$ |                | 44<br>16<br>13 | 150<br>30<br>26 |            | 190<br>38<br>33 |             | 225<br>45<br>38 | ns              | 2.0<br>4.5<br>6.0 | Fig.7           |
| $t_{THL}/t_{TLH}$ | output transition time  |                | 14<br>5<br>4   | 60<br>12<br>10  |            | 75<br>15<br>13  |             | 90<br>18<br>15  | ns              | 2.0<br>4.5<br>6.0 | Fig.5 and Fig.6 |

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## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see *"74HC/HCT/HCU/HCMOS Logic Family Specifications"*.

Output capability: bus driver

I<sub>CC</sub> category: MSI

### Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications. To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT           | UNIT LOAD COEFFICIENT |
|-----------------|-----------------------|
| A <sub>n</sub>  | 1.50                  |
| B <sub>n</sub>  | 0.40                  |
| $\overline{OE}$ | 1.50                  |
| DIR             | 0.90                  |

## AC CHARACTERISTICS FOR 74HCT

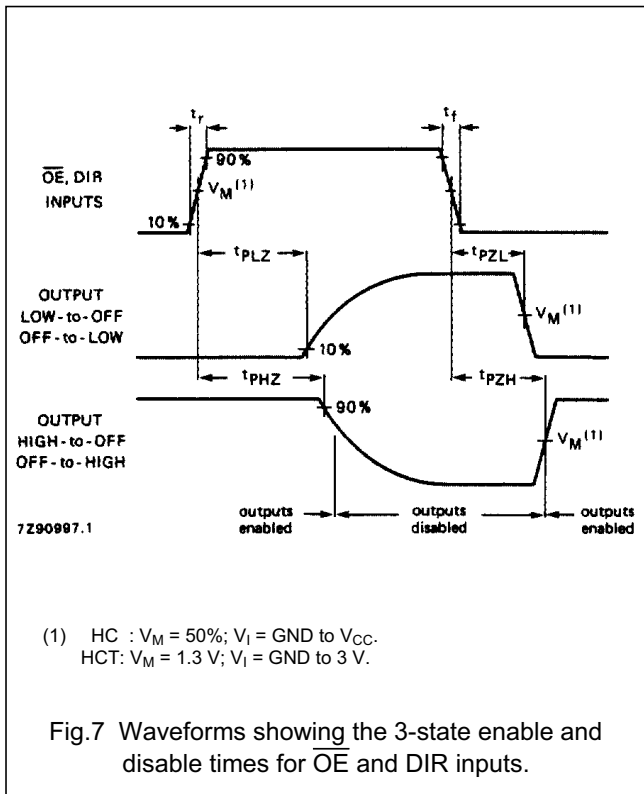
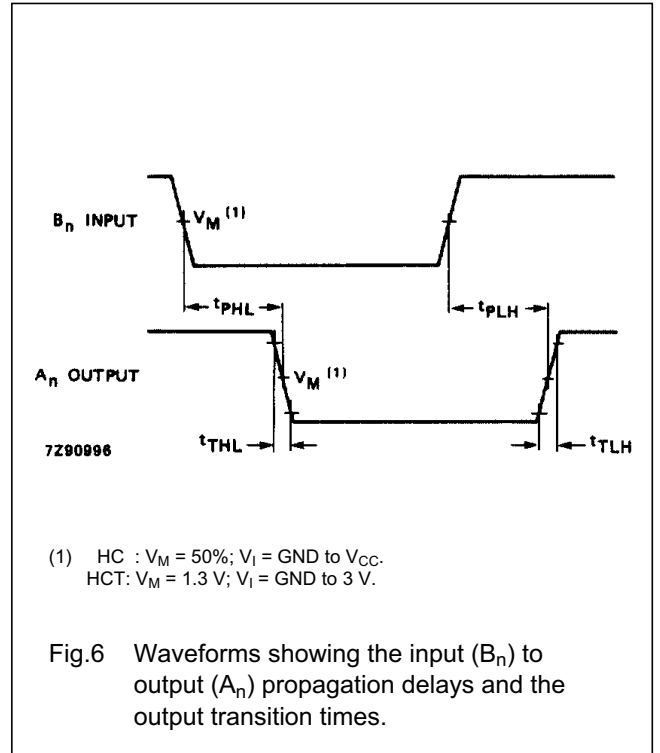
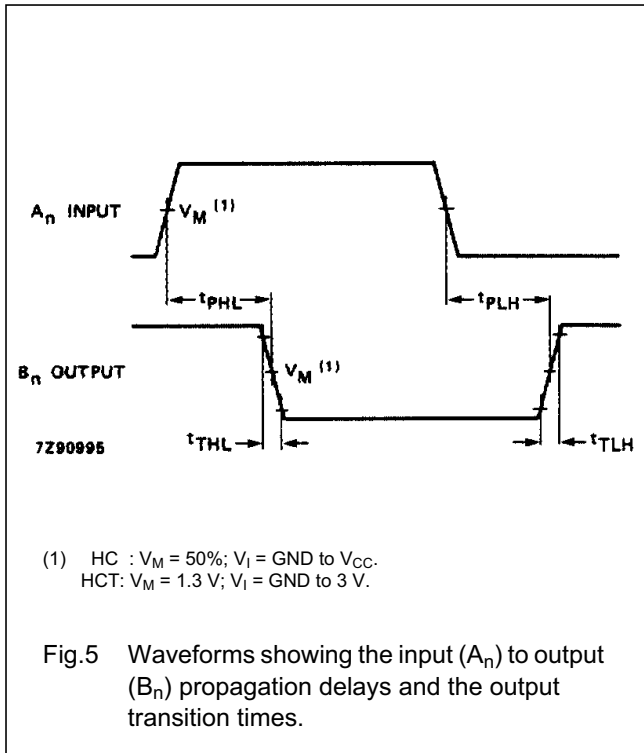
GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

| SYMBOL                              | PARAMETER   | T <sub>amb</sub> (°C) |      |      |            |      |             | UNIT | TEST CONDITIONS        |           |                 |
|-------------------------------------|---|-----------------------|------|------|------------|------|-------------|------|------------------------|-----------|-----------------|
|                                     |   | 74HCT                 |      |      |            |      |             |      | V <sub>CC</sub><br>(V) | WAVEFORMS |                 |
|                                     |   | +25                   |      |      | -40 to +85 |      | -40 to +125 |      |                        |           |                 |
|                                     |   | min.                  | typ. | max. | min.       | max. | min.        |      |                        |           | max.            |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>A <sub>n</sub> to B <sub>n</sub> ;<br>inverting  |                       | 10   | 20   |            | 25   |             | 30   | ns                     | 4.5       | Fig.5           |
| t <sub>PHL</sub> / t <sub>PLH</sub> | propagation delay<br>B <sub>n</sub> to A <sub>n</sub> ;<br>non-inverting (true)                                     |                       | 13   | 23   |            | 29   |             | 35   | ns                     | 4.5       | Fig.6           |
| t <sub>PZH</sub> / t <sub>PZL</sub> | 3-state output enable time<br>$\overline{OE}$ , DIR to A <sub>n</sub> ;<br>$\overline{OE}$ , DIR to B <sub>n</sub>  |                       | 16   | 30   |            | 38   |             | 45   | ns                     | 4.5       | Fig.7           |
| t <sub>PHZ</sub> / t <sub>PLZ</sub> | 3-state output disable time<br>$\overline{OE}$ , DIR to A <sub>n</sub> ;<br>$\overline{OE}$ , DIR to B <sub>n</sub> |                       | 17   | 30   |            | 38   |             | 45   | ns                     | 4.5       | Fig.7           |
| t <sub>THL</sub> / t <sub>TLH</sub> | output transition time  |                       | 5    | 12   |            | 15   |             | 18   | ns                     | 4.5       | Fig.5 and Fig.6 |

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AC WAVEFORMS



PACKAGE OUTLINES

See "74HC/HCT/HCU/HCMOS Logic Package Outlines".