

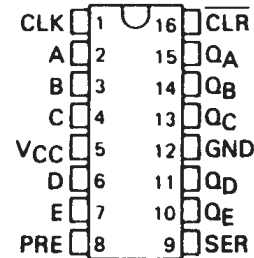
SN5496, SN54LS96, SN7496, SN74LS96 5-BIT SHIFT REGISTERS

SDLS946 - MARCH 1974 - REVISED MARCH 1988

- N-Bit Serial-To-Parallel Converter
- N-Bit Parallel-To-Serial Converter
- N-Bit Storage Register

SN5496, SN54LS96 . . . J OR W PACKAGE
SN7496 . . . N PACKAGE
SN74LS96 . . . D OR N PACKAGE
(TOP VIEW)

TYPE	TYPICAL	
	PROPAGATION DELAY TIME	POWER DISSIPATION
'96	25 ns	240 mW
'LS96	25 ns	60 mW



description

These shift registers consist of five R-S master-slave flip-flops connected to perform parallel-to-serial or serial-to-parallel conversion of binary data. Since both inputs and outputs for all flip-flops are accessible, parallel-in/parallel-out or serial-in/serial-out operation may be performed.

All flip-flops are simultaneously set to a low output level by applying a low-level voltage to the clear input while the preset is inactive (low). Clearing is independent of the level of the clock input.

The register may be parallel loaded by using the clear input in conjunction with the preset inputs. After clearing all stages to low output levels, data to be loaded is applied to the individual preset inputs (A, B, C, D, and E) and a high-level load pulse is applied to the preset enable input. Presetting like clearing is independent of the level of the clock input.

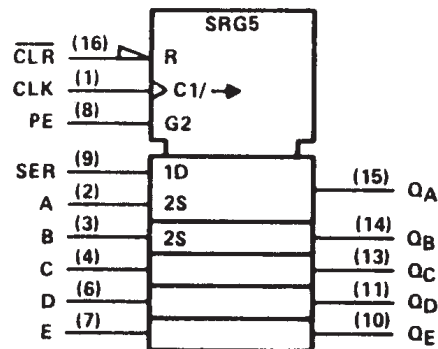
Transfer of information to the outputs occurs on the positive-going edge of the clock pulse. The proper information must be set up at the R-S inputs of each flip-flop prior to the rising edge of the clock input waveform. The serial input provides this information to the first flip-flop, while the outputs of the subsequent flip-flops provide information for the remaining R-S inputs. The clear input must be high and the preset or preset enable inputs must be low when clocking occurs.

FUNCTION TABLE

CLEAR	PRESET					CLOCK	SERIAL	OUTPUTS				
	ENABLE	A	B	C	D			E	Q _A	Q _B	Q _C	Q _D
L	L	X	X	X	X	X	X	L	L	L	L	L
L	X	L	L	L	L	X	X	L	L	L	L	L
H	H	H	H	H	H	X	X	H	H	H	H	H
H	H	L	L	L	L	L	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}
H	H	H	L	H	L	H	X	H	Q _{B0}	H	Q _{D0}	H
H	L	X	X	X	X	L	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}
H	L	X	X	X	X	↑	H	H	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}
H	L	X	X	X	X	↑	L	L	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}

H = high level (steady state), L = low level (steady state)
X = irrelevant (any input, including transition)
↑ = transition from low to high level
Q_{A0}, Q_{B0}, etc. = the level of Q_A, Q_B, etc. respectively before the indicated steady-state input conditions were established.
Q_{An}, Q_{Bn}, etc. = the level of Q_A, Q_B, etc. respectively before the most recent ↑ transition of the clock.

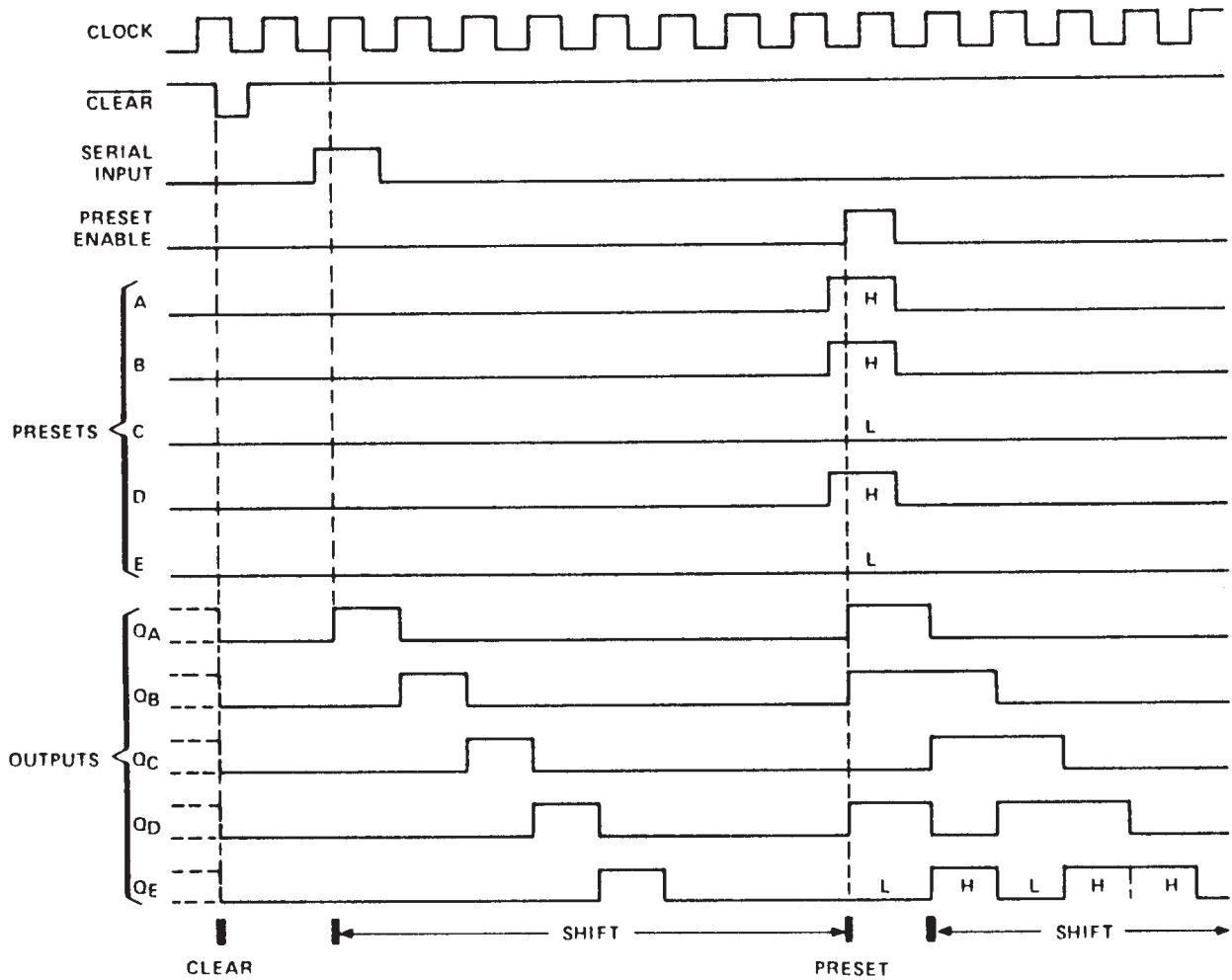
logic symbol[†]



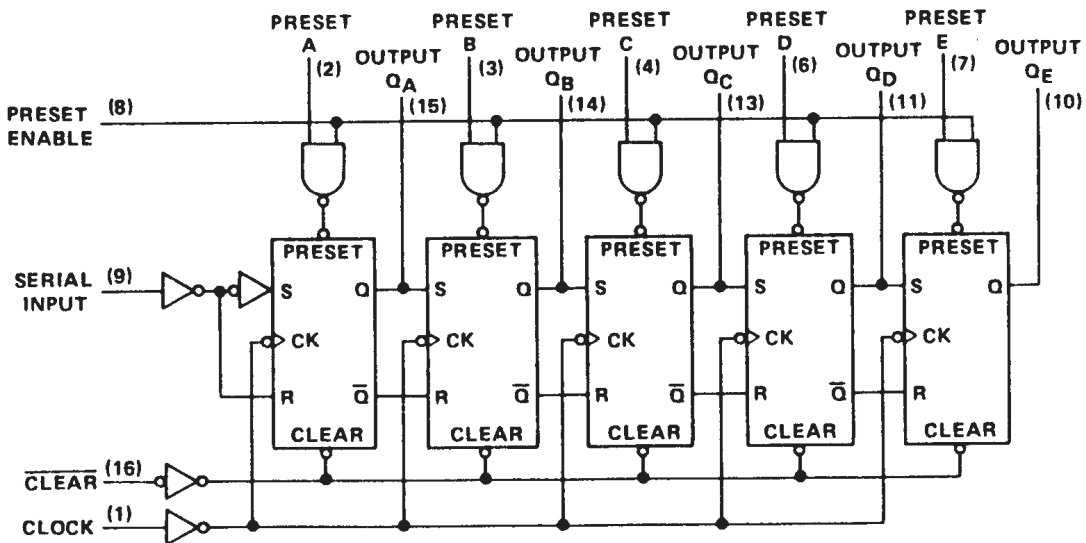
[†]This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

**SN5496, SN54LS96,
SN7496, SN74LS96
5-BIT SHIFT REGISTERS**

typical clear, shift, preset, and shift sequences

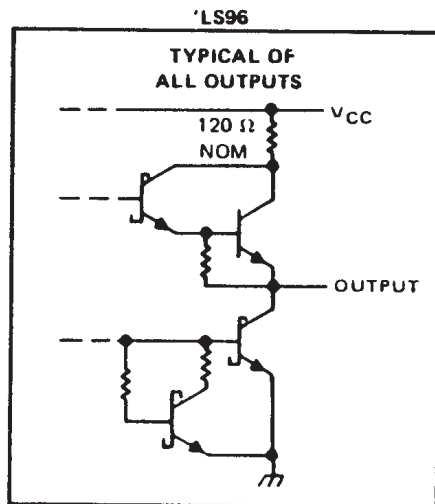
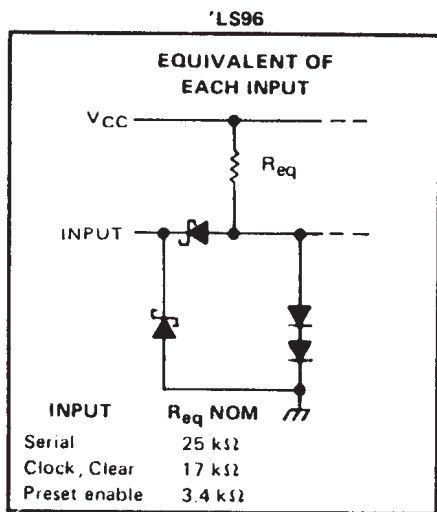
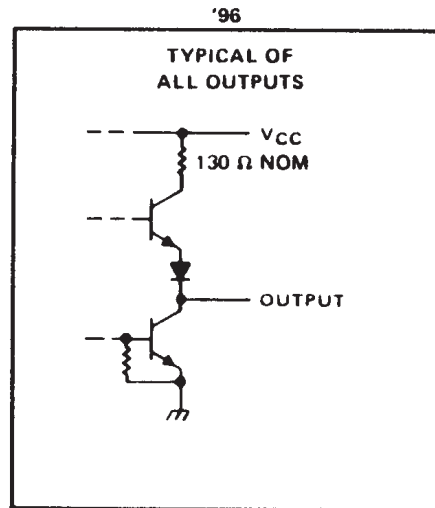
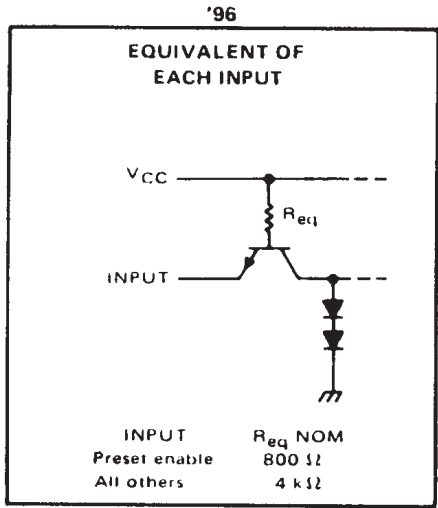


logic diagram (positive logic)



**SN5496, SN54LS96,
SN7496, SN74LS96
5-BIT SHIFT REGISTERS**

schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 2): '96	5.5 V
'LS96	7 V
Operating free-air temperature: SN54'	-55°C to 125°C
SN74'	0°C to 70°C
Storage temperature range	-65°C to 150°C

- NOTES: 1. Voltage values are with respect to network ground terminal.
2. Input voltage must be zero or positive with respect to network ground terminal.

SN5496, SN7496 5-BIT REGISTERS

recommended operating conditions

	SN5496			SN7496			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			16			16	mA
Clock frequency, f_{clock}	0		10	0		10	MHz
Width of clock input pulse, $t_w(\text{clock})$	35			35			ns
Width of preset and clear input pulse, t_w	30			30			ns
Serial input setup time, t_{SU} (see Figure 1)	30			30			ns
Serial input hold time, t_h (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN5496			SN7496			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.8			0.8	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2\text{ V}$, $V_{IL} = 0.8\text{ V}$, $I_{OH} = -400\ \mu\text{A}$	2.4	3.4		2.4	3.4		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN}$, $V_{IH} = 2\text{ V}$, $V_{IL} = 0.8\text{ V}$, $I_{OL} = 16\text{ mA}$		0.2	0.4		0.2	0.4	V
I_I	Input current at maximum input voltage	$V_{CC} = \text{MAX}$, $V_I = 5.5\text{ V}$			1			1	mA
I_{IH}	High-level input current	any input except preset enable			40			40	μ A
		preset enable			200			200	
I_{IL}	Low-level input current	any input except preset enable			-1.6			-1.6	mA
		preset enable			-8			-8	
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX}$	-20		-57	-18		-57	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX}$, See Note 3		48	68		48	79	mA

† For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5\text{ V}$, $T_A = 25^{\circ}\text{C}$.

§ Not more than one output should be shorted at a time.

NOTE 3: I_{CC} is measured with the clear input grounded and all other inputs and outputs open.

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output from clock		25	40	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clock		25	40	ns
t_{PLH}	Propagation delay time, low-to-high-level output from preset or preset enable		28	35	ns
t_{PHL}	Propagation delay time, high-to-low-level output from clear			55	ns

SN54LS96, SN74LS96

5-BIT SHIFT REGISTERS

recommended operating conditions

	SN54LS96			SN74LS96			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μ A
Low-level output current, I_{OL}			4			8	mA
Clock frequency, f_{clock}	0		25	0		25	MHz
Width of clock input pulse, $t_{W(clock)}$	20			20			ns
Width of preset and clear input pulse, t_W	30			30			ns
Serial input setup time, t_{setup} (see Figure 1)	30			30			ns
Serial input hold time, t_{hold} (see Figure 1)	0			0			ns
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}$ C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†	SN54LS96			SN74LS96			UNIT
			MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage		2			2			V
V_{IL}	Low-level input voltage				0.7			0.8	V
V_{IK}	Input clamp voltage	$V_{CC} = \text{MIN.}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH}	High-level output voltage	$V_{CC} = \text{MIN.}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}, I_{OH} = -400 \mu\text{A}$	2.5	3.5		2.7	3.5		V
V_{OL}	Low-level output voltage	$V_{CC} = \text{MIN.}, V_{IH} = 2 \text{ V}, V_{IL} = V_{IL \text{ max}}$	$I_{OL} = 4 \text{ mA}$		0.25	0.4	0.25	0.4	V
			$I_{OL} = 8 \text{ mA}$				0.35	0.5	
I_I	Input current at maximum input voltage	Preset enable	$V_{CC} = \text{MAX.}, V_I = 7 \text{ V}$			0.5			mA
		All others				0.1			
I_{IH}	High-level input current	Preset enable	$V_{CC} = \text{MAX.}, V_I = 2.7 \text{ V}$			100			μ A
		All others				20			
I_{IL}	Low-level input current	Preset enable	$V_{CC} = \text{MAX.}, V_I = 0.4 \text{ V}$			-2			mA
		All others				-0.4			
I_{OS}	Short-circuit output current§	$V_{CC} = \text{MAX.}$	-20		-100	-20		-100	mA
I_{CC}	Supply current	$V_{CC} = \text{MAX.},$ See Note 3	12	20		12	20		mA

† For conditions shown at MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 3: I_{CC} is measured with the clear input grounded and all other inputs and outputs open.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^{\circ}\text{C}$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH} Propagation delay time, low-to-high-level output from clock	$C_L = 15 \text{ pF}, R_L = 2 \text{ k}\Omega,$ See Figure 1		25	40	ns
t_{PHL} Propagation delay time, high-to-low-level output from clock			25	40	ns
t_{PLH} Propagation delay time, low-to-high-level output from preset or preset enable			28	35	ns
t_{PHL} Propagation delay time, high-to-low-level output from clear				55	ns

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN5496J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN7496N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS96D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74LS96DR	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74LS96J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SN74LS96N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS96N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SNJ5496J	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI
SNJ5496W	OBSOLETE	CFP	W	16		TBD	Call TI	Call TI

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

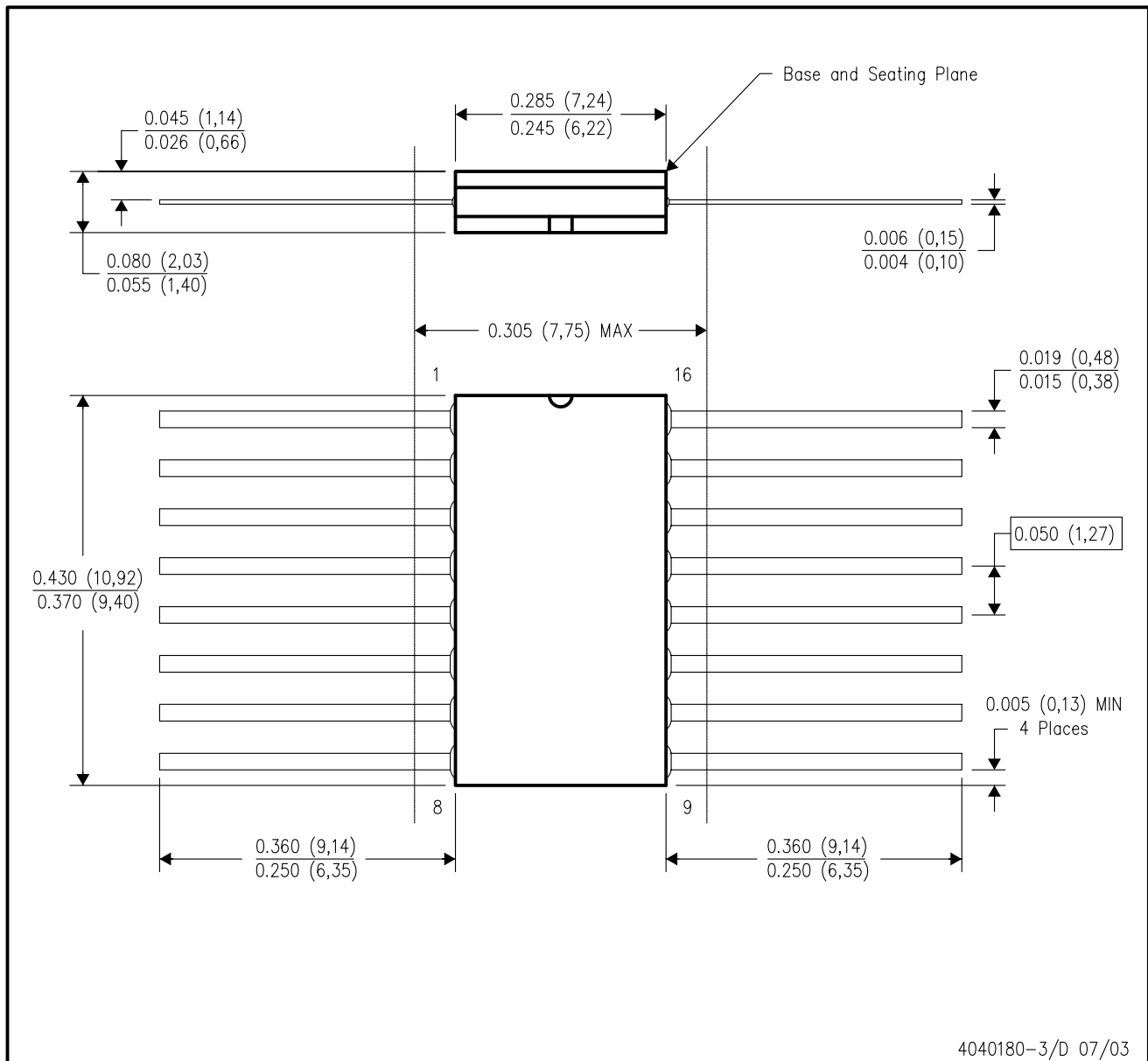
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer:The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

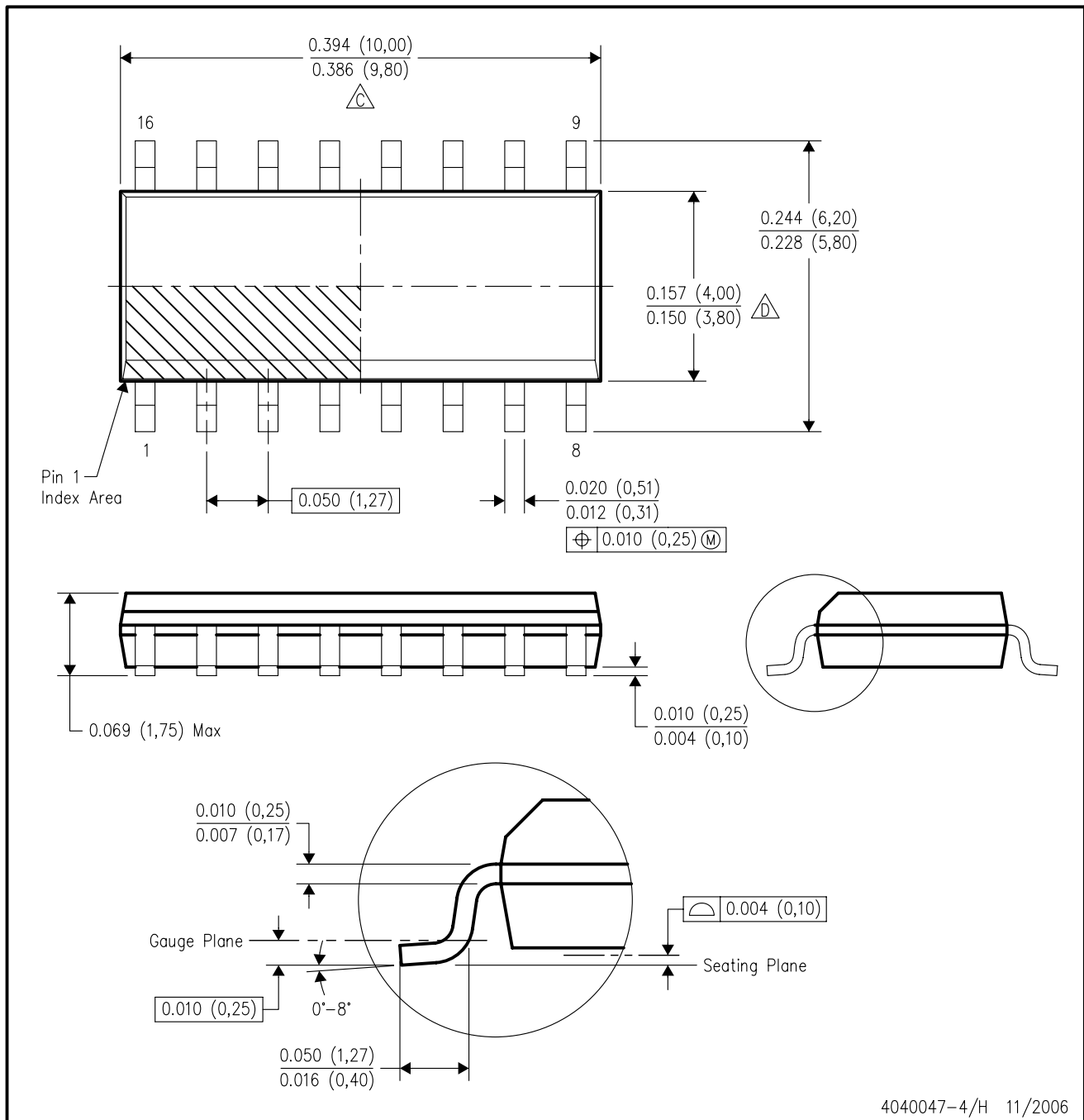
16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/H 11/2006

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AC.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products

Amplifiers	amplifier.ti.com
Data Converters	dataconverter.ti.com
DSP	dsp.ti.com
Interface	interface.ti.com
Logic	logic.ti.com
Power Mgmt	power.ti.com
Microcontrollers	microcontroller.ti.com
Low Power Wireless	www.ti.com/lpw

Applications

Audio	www.ti.com/audio
Automotive	www.ti.com/automotive
Broadband	www.ti.com/broadband
Digital Control	www.ti.com/digitalcontrol
Military	www.ti.com/military
Optical Networking	www.ti.com/opticalnetwork
Security	www.ti.com/security
Telephony	www.ti.com/telephony
Video & Imaging	www.ti.com/video
Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265