

100 mA Adjustable Output Positive Voltage Regulator

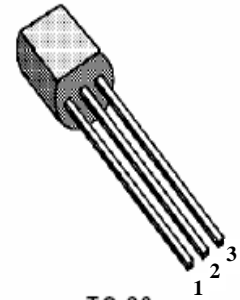
LM317

The LM317 is an adjustable 3-terminal positive voltage regulator capable of supplying in excess of 100 mA over an output voltage range of 1.2 V to 37 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage. Further, it employs internal current limiting, thermal shutdown and safe area compensation, making them essentially blow – out proof.

The LM317 serves a wide variety of applications including local, on card regulation. This device can also be used to make a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM317 can be used as a precision current regulator.

Features

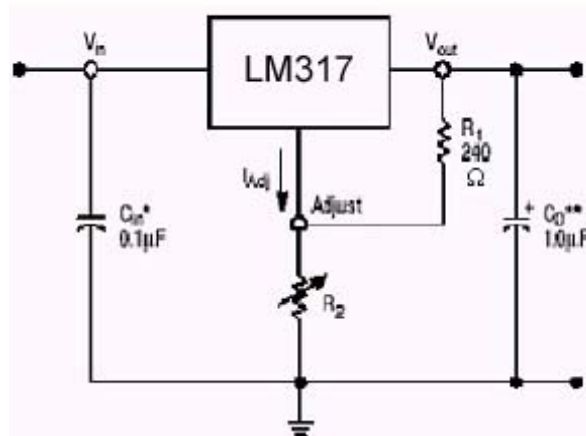
- Output Current in Excess of 100 mA
- Output Adjustable Between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short Circuit Current Limiting
- Output Transistor Safe-Area Compensation
- Floating Operation for High Voltage Applications
- Standard 3-Lead Transistor Package
- Eliminates Stocking Many Fixed Voltages



TO-92

Pin 1. Adjust
2. Vout
3. Vin

Simplified Application



*Cin is required if regulator is located an appreciable distance from power supply filter.

**Co is not needed for stability, however, it does improve transient response.

$$V_{out} = 1.25 V (1 + R_2/R_1) + I_{adj}R_2$$

Since I_{adj} is controlled to less than 100µA, the error associated with this term is negligible in most applications.

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input-Output Differential	$V_I - V_O$	40	Vdc
Power Dissipation Case TO-92 $T_A = 25^\circ\text{C}$	P_D	Internally Limited	W
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	160	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Case Case SOIC-8 (Note 1) $T_A = 25^\circ\text{C}$	$R_{\theta JC}$	83	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	180	$^\circ\text{C/W}$
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	45	$^\circ\text{C/W}$
Operating Junction Temperature Range	T_j	-10 to +125	$^\circ\text{C}$
Storage Temperature Range	T_{stg}	-65 to +150	$^\circ\text{C}$

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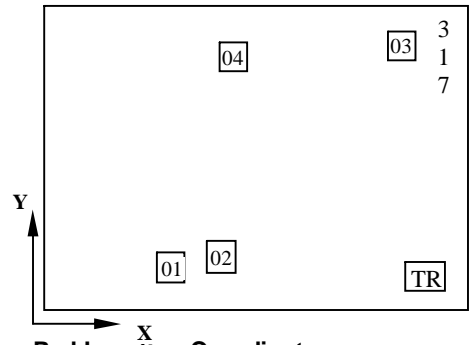
LM317 (Chip)

ELECTRICAL CHARACTERISTICS

($V_I - V_O = 5.0\text{ V}$; $I_O = 40\text{ mA}$; $T_A = 25^\circ\text{C}$, unless otherwise noted, I_{max} and P_{max} (NOTE1))

Characteristics	Symbol	Min	Max	Unit
Reference Voltage ($T_A = -10^\circ$ to $+125^\circ\text{C}$) $3.0\text{ V} \leq V_I - V_O \leq 40\text{ V}$, $10\text{ mA} \leq I_O \leq I_{max}, P_D \leq P_{max}$	V_O	1.20	1.30	V
Line Regulation (NOTE2) $3.0\text{ V} \leq V_I - V_O \leq 40\text{ V}$, $I_O = 5\text{ mA}$	ΔV_{ov}	-	20	mV
Line Regulation ($T_A = -10^\circ$ to $+125^\circ\text{C}$) (NOTE2) $3.0\text{ V} \leq V_I - V_O \leq 40\text{ V}$, $I_O = 5\text{ mA}$	ΔV_{ov}	-	35	mV
Load Regulation (NOTE2) $10\text{ mA} \leq I_O \leq I_{max}, V_I = 6.25\text{ V}$	ΔV_{oi}	-	6.25	mV
Load Regulation ($T_A = -10^\circ$ to $+125^\circ\text{C}$) (NOTE2) $10\text{ mA} \leq I_O \leq I_{max}, V_I = 6.25\text{ V}$	ΔV_{oi}	-	18.75	mV
Adjustment Pin Current	I_{Adj}	10	100	μA
Adjustment Pin Current Change, $P_D \leq P_{max}$ $3.0\text{ V} \leq V_I - V_O \leq 40\text{ V}$, $10\text{ mA} \leq I_O \leq I_{max}$	ΔI_{Adj}	-	5	μA
Maximum Output Current, $P_D \leq P_{max}$	$I_{O\text{ MAX}}$	0.1	-	A
Minimum Load Current to Maintain Regulation ($V_I - V_O = 40\text{ V}$)	$I_{L\text{ min}}$	-	5	mA
Ripple Rejection $V_O = 1.2\text{ V}$, $f = 120\text{ Hz}$	RR	60	-	dB

Pad Layout



Pad Location Coordinates

Pad #	X (μm)	Y (μm)	Pad names	PIN #
01	375	92	Output	2
02	545	110	Input	3
03	126 2	735	Adjustable	1
04	570	690	Output	2

NOTES:

- $I_{max} = 100\text{ mA}$, $P_{max} = 625\text{ mW}$
- Load and line regulation are specified at constant junction temperature. Changes in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.

Physical Characteristics:

- ◆ Wafer Diameter 100 \pm 0.5 mm
- ◆ Wafer thickness^(*) 280 \pm 20 μm
- ◆ Die size 1.53 x 0.93 mm²
- ◆ Scribe width 100 μm
- ◆ Passivation PSG

*The wafer thickness shall be specified in a PO or Contract

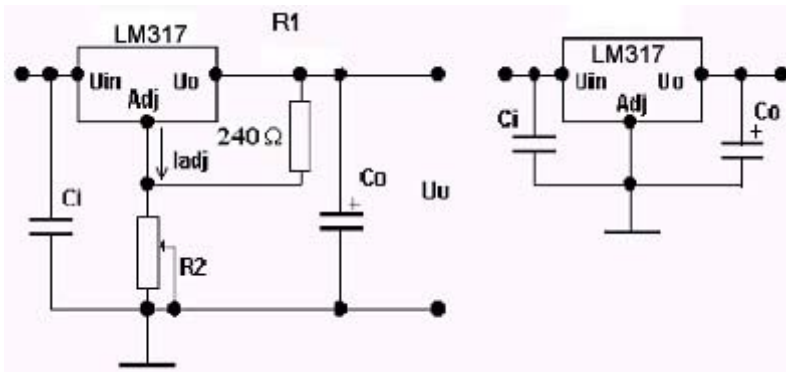


Fig.1 Test Circuit for $V_O > 1.25\text{ V}$
 $C_i = 0,1\mu\text{F}$, $C_o = 1,0\mu\text{F}$.
 $V_O = 1,25(1 + R_2/R_1)I_{ADJ} R_2$

Fig.2 Test Circuit for $V_O = 1.25\text{ V}$
 $C_i = 0,1\mu\text{F}$, $C_o = 1,0\mu\text{F}$.

Bonding Diagram (TO-92)

