

Silicon NPN Power Transistors

BDX65C

DESCRIPTION

- With TO-3 package
- DARLINGTON
- Complement to type BDX64C

APPLICATIONS

- Designed for power amplification and switching applications.

PINNING (See Fig.2)

PIN	DESCRIPTION
1	Base
2	Emitter
3	Collector

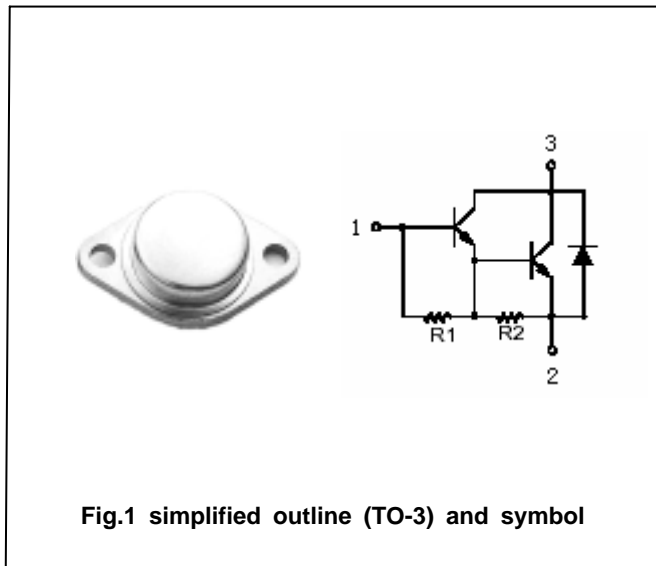


Fig.1 simplified outline (TO-3) and symbol

Absolute maximum ratings(Ta=25 )

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
V <sub>CBO</sub>	Collector-base voltage	Open emitter	120	V
V <sub>CEO</sub>	Collector-emitter voltage	Open base	120	V
V <sub>EBO</sub>	Emitter-base voltage	Open collector	5	V
I <sub>C</sub>	Collector current		12	A
I <sub>CM</sub>	Collector current(peak)		16	A
I <sub>B</sub>	Base current		0.2	A
P <sub>T</sub>	Total power dissipation	T <sub>C</sub> =25	117	W
T <sub>j</sub>	Junction temperature		-55~200	
T <sub>stg</sub>	Storage temperature		-55~200	

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	MAX	UNIT
R <sub>th j-c</sub>	Thermal resistance from junction to case	1.5	/W

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## CHARACTERISTICS

T<sub>j</sub>=25 unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNIT
V <sub>CEO(SUS)</sub>	Collector-emitter sustaining voltage	I <sub>C</sub> =0.1A ; I <sub>B</sub> =0; L=25mH	120			V
V <sub>CEsat</sub>	Collector-emitter saturation voltage	I <sub>C</sub> =5A ; I <sub>B</sub> =20mA			2	V
V <sub>BE</sub>	Base-emitter voltage	I <sub>C</sub> =5A; V <sub>CE</sub> =3V			3	V
I <sub>CBO</sub>	Collector cut-off current	V <sub>CB</sub> =120V; I <sub>E</sub> =0 T <sub>C</sub> =150			0.4 3	mA
I <sub>CEO</sub>	Collector cut-off current	V <sub>CE</sub> =60V; I <sub>B</sub> =0			1	mA
I <sub>EBO</sub>	Emitter cut-off current	V <sub>EB</sub> =5V; I <sub>C</sub> =0			5	mA
V <sub>F</sub>	Diode forward voltage	I <sub>F</sub> =3A		1.8		V
h <sub>FE-1</sub>	DC current gain	I <sub>C</sub> =1A ; V <sub>CE</sub> =3V		1500		
h <sub>FE-2</sub>	DC current gain	I <sub>C</sub> =5A ; V <sub>CE</sub> =3V	1000			
h <sub>FE-3</sub>	DC current gain	I <sub>C</sub> =10A ; V <sub>CE</sub> =3V		1500		
f <sub>T</sub>	Transition frequency	I <sub>C</sub> =5A ; V <sub>CE</sub> =3V		7		MHz

PACKAGE OUTLINE

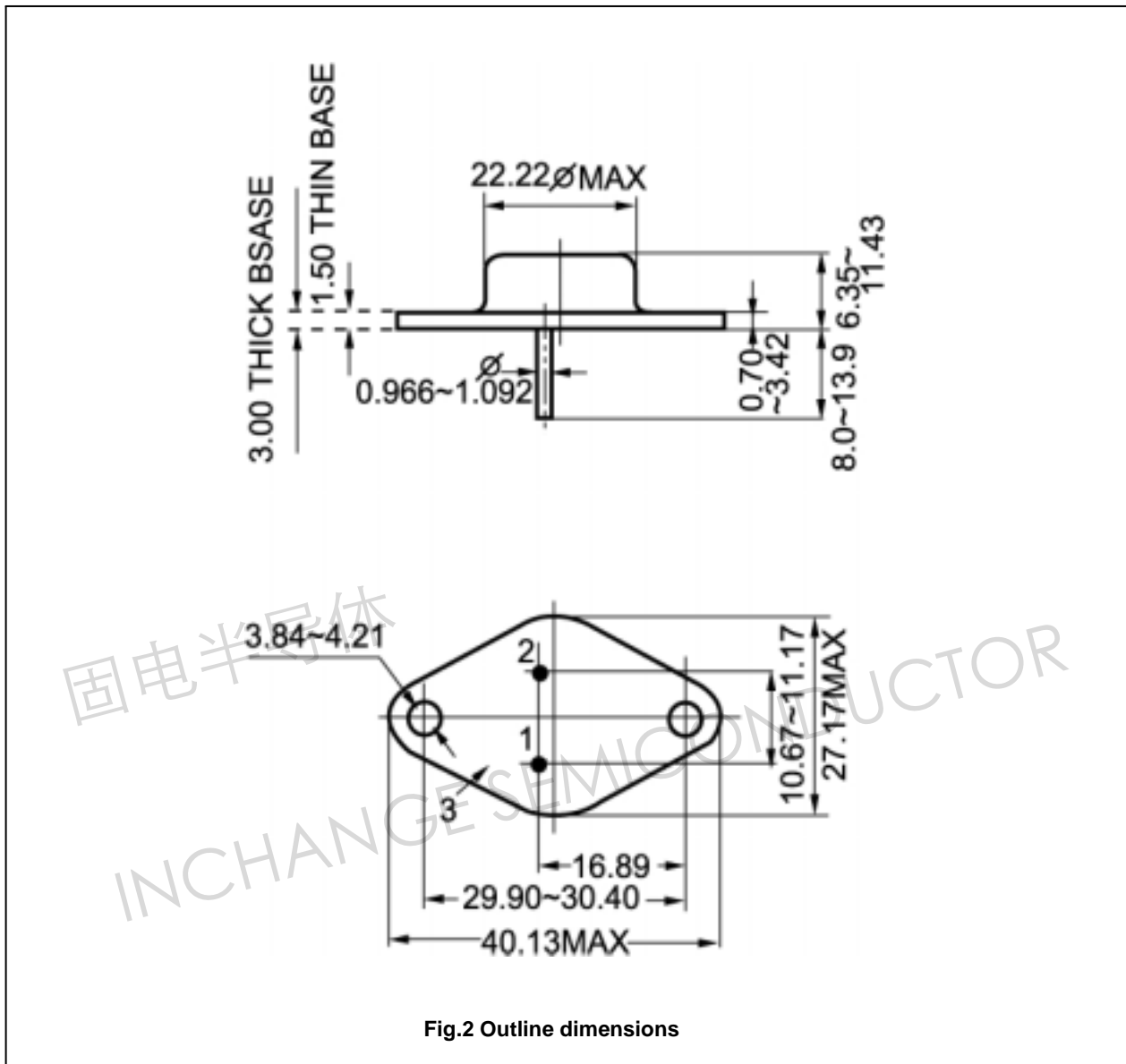


Fig.2 Outline dimensions