

Product Preview
System 4 Improved Stereoton
Single Chip TV Sound Control

This single chip performs all the necessary functions for sound control required in a TV receiver in accordance with German standard transmission mode, with NICAM transmission mode, and SECAM transmission mode.

The MC44131 is manufactured in a single chip using Motorola's CMOS process and is an improved version of the MC44130.

- Application: Audio for European Televisions
- Part of Motorola System 4
- Fully Controlled Through IIC Bus
- Accepts Base Band Dual Carrier Signals or NICAM Decoded Signals or SECAM Decoded Signals
- "Pilot Tone" Demodulation and Identification
- Mono, Stereo, Dual Language Processing
- Maximum Stereo Separation Control
- Volume, Treble, and Bass Control
- Special Effects: Pseudo and Extra Wide Stereo
- Mute and Separate Power-On Reset Mute
- Loudspeaker, Headphone, HIFI Outputs
- Peripheral (SCART) Input/Output
- Independent Volume Control Left/Right on Loudspeaker and on Headphone Outputs
- Mono Recorder Drive Capability
- New Switching Matrix Allows 31 Signal Routing Options
- Auxiliary Attenuator to Avoid Clipping when Bass is Boosted

The MC44131 is an improved version of the popular MC44130. It combines all following functions in a 28-pin DIP package:

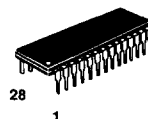
- Pilot Tone Decoding
- Baseband Stereo Signal Decoding
- Signal De-Emphasis
- Direct Balance Adjustment via Software (Set-Up)
- IIC Bus Controlled Routing of Baseband/Monaural/SCART Inputs to Loudspeaker/Headphone/HIFI/SCART Outputs
- Loudspeaker Output Control (Tone, Special Effects, Independent Volume Control Left/Right)
- Headphone Output Control (Independent Volume Control Left/Right)
- Re-Creation of MONO Output on SCART for Mono Recorders

MC44131 has improved MC44130 performances in the following areas:

- Crosstalk Figures
- Enhanced Drive Capability on SCART Output
- Lowered Output Impedance on SCART Output
- Reduced Sensitivity for Identification about 25%
- Introduced Latch on I2C Identification Interface
- New Switching Matrix for Independent Signal Routing (31 Options)
- Auxiliary Attenuator on Front End of Tone Control to Fix Clipping when Bass is Boosted
- Reduced Audio Signal Routing Losses
- Shorter Charge-Up Time on Analog Ground Pin

This document contains information on a product under development. Motorola reserves the right to change or discontinue this product without notice.

MC44131



P SUFFIX
PLASTIC PACKAGE
CASE 710-02

ORDERING INFORMATION

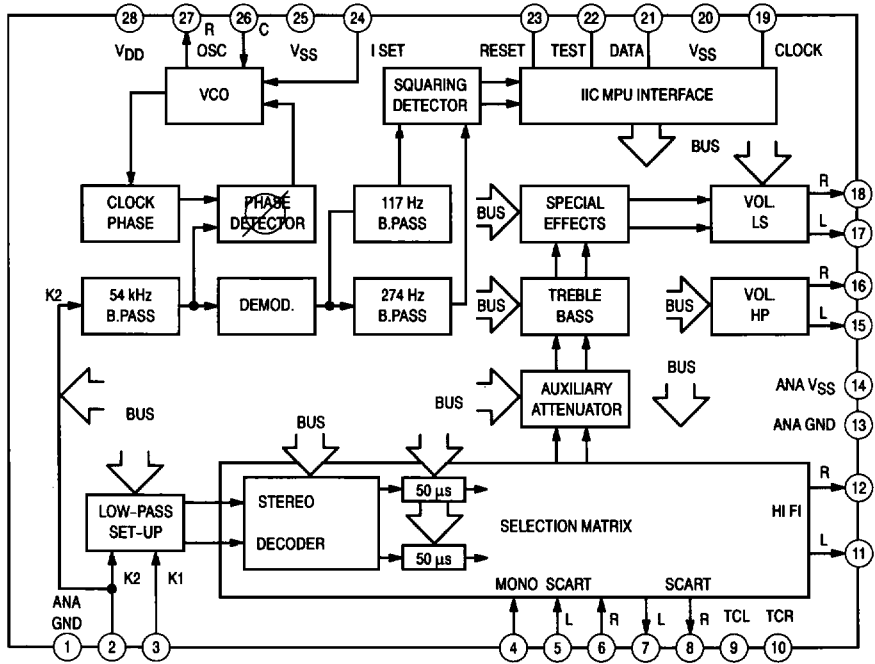
MC44131P DIP

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PIN ASSIGNMENT

ANA GND	1	28	V _{DD}
K2	2	27	OSC R
K1	3	26	OSC C
MONO IN	4	25	V _{SS}
SCART IN L	5	24	I SET
SCART IN R	6	23	RESET
SCART OUT L	7	22	TEST
SCART OUT R	8	21	DATA
TC L	9	20	V _{SS}
TC R	10	19	CLOCK
HIFI L	11	18	LS R
HIFI R	12	17	LS L
ANA GND	13	16	HP R
ANA V _{SS}	14	15	HP L

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Characteristic	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	- 0.5 to + 15	V
Operating Temperature Range	T_A	0 to 70	°C
Storage Temperature	T_{stg}	- 40 to + 125	°C

NOTE: Default conditions (unless otherwise specified):

- All tests performed as per Figure 1.
- 1% accuracy resistors — resonator Murata CSB437F3 ($f_s = 427$ kHz, $f_p = 464$ kHz, C_{stat} at kHz = 630 pF, $R_s = 30$ Ω). $V_{DD} = 12$ V, $T_A = 25^\circ\text{C}$.
- V_a amplitude is 500 mVrms, V_a frequency is 1 kHz, V_r amplitude is 400 mVpp, V_r frequency is 1 kHz, V_p frequency is 54.6875 kHz with or without amplitude modulation.
- Values for subaddress, data, and read bits have to be understood as hexadecimal values.
- Treble/Bass: fiat = subaddress 05 data 88.
- Volumes HP and LS: Max. = subaddress 01, 02, 03, 04 data 00.
- K1, K2 Set-Up: Midrange = subaddress 00, 07 data 20.
- Demute, matrix option 00, no special effects = subaddress 06 data 00.
- When switches are not mentioned, they are considered as OFF.
- Pin 22 is not connected or is connected to Pin 20.

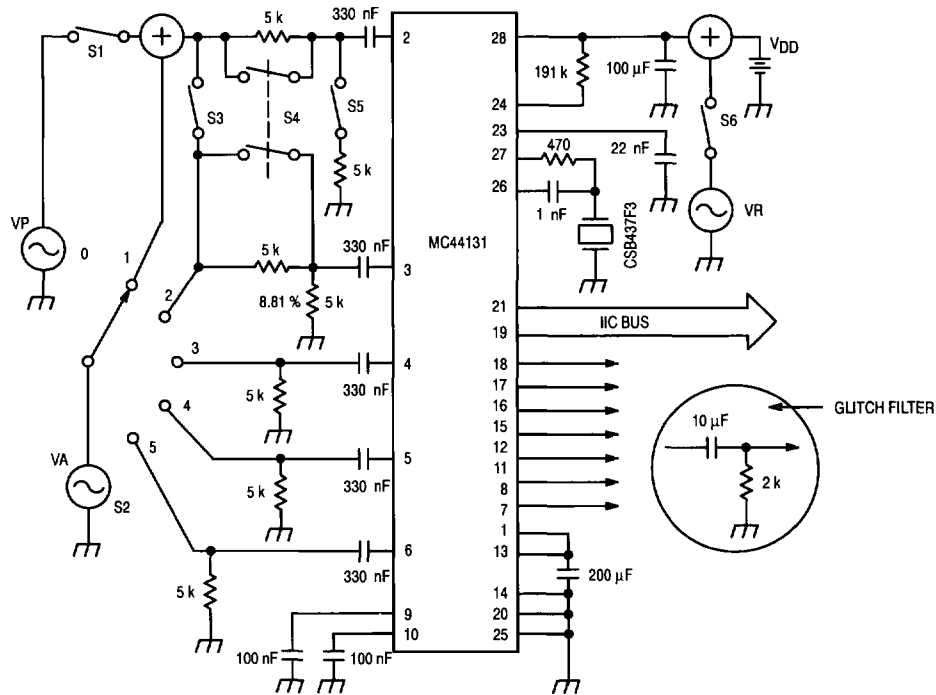


Figure 1. Device Under Test

POWER SUPPLY

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Unit
Power Supply Voltage	V _{DD}	28		10.8	12	13.2	V
Power Supply Current	I _{DD}	28		—	35	60	mA

OSCILLATOR

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Unit
Free Running Frequency	FOSC	27	Decoder and de-emphasis switched OFF	430	437.5	450	kHz

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IDENTIFICATION

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Unit
Minimum Modulation	LMPA	2, 27, 19, 21	Pilot amplitude from 50 mVpp to 500 mVpp before AM modulation (see also Note 2)	—	30	40	%
Maximum Modulation				60	—	—	%

VOLUME CONTROLS

Left and right outputs may be balanced at any level to within half step size by independent control of left/right side attenuators.

LOUDSPEAKER (See Note)

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Unit
Step Size from Step 0 to Step 50*	LSSS	6, 17, 18	Subaddr. 01, 02 Data n → V _{out} (n) Subaddr. 01, 02, Data n+1 → V _{out} (n+1) LSSS = $20 \log (V_{out}(n)/V_{out}(n+1))$	0	1.25	2.5	dB
Depth from Step 0 to Step 50*	LSDL	6, 17, 18	Subaddr. 01, 02 Data 32 → V _{out} (32) LSDL = $20 \log (V_{out}(0)/V_{out}(32))$	55	60	70	dB
Depth at Step 62*	LSDL	6, 17, 18	Subaddr. 01, 02 Data 3E → V _{out} (3E) LSDL = $20 \log (V_{out}(0)/V_{out}(3E))$	65	—	—	dB

NOTE: For all loudspeaker volume control tests, channel left and right are at the same step. Subaddress 06 data 01, S2 = 5.

* Step values understood as decimal values.

HEADPHONE (See Note)

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Unit
Step Size from Step 0 to Step 25*	HPSS	5, 15, 16	Subaddr. 03, 04 Data n → V _{out} (n) Subaddr. 03, 04 Data n+1 → V _{out} (n+1) HPSS = $20 \log (V_{out}(n)/V_{out}(n+1))$	0	2.5	4.0	dB
Depth from Step 0 to Step 25*	HPDP	5, 15, 16	Subaddr. 03, 04 Data 00 → V _{out} (00) HPDP = $20 \log (V_{out}(00)/V_{out}(19))$	55	60	70	dB
Depth at Step 30*	HPDP	5, 15, 16	Subaddr. 03, 04 Data 1E → V _{out} (E) HPDP = $20 \log (V_{out}(0)/V_{out}(1E))$	60	—	—	dB

NOTE: For all headphone volume control tests, channel left and right are at the same step. Subaddress 06 data 01, S2 = 4.

* Step values understood as decimal values.

K1, K2 SET-UP CONTROL (See Note)

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Unit
Control Range	SUD	2, 3, 7, 8	Subaddr. 06, Data: 05 Subaddr. 00, 07 Data: 3E $V_{out}(3E)$ Subaddr. 00, 07 Data: 00 $V_{out}(00)$ $SUD = 20 \log (V_{out}(3E)/V_{out}(00)) $	3.5	4.5	5.5	dB
Step Size K2	SSK2	2, 3, 8	Subaddr. 06, Data: 05 Subaddr. 07, Data: 00 ... 3F	0	0.1	0.2	dB
Step Size K1	SSK1	2, 3, 7	Subaddr. 06, Data: 05 Subaddr. 00, Data: 00, 02 ... 3E	0	0.2	0.4	dB
Stereo Separation Set-Up at K1/K2 Mid.	SUSM	2, 3, 7, 8	Subaddr. 06, Data: 00 Subaddr. 00, 07, Data: 20 V_{outL} on Pin 7, V_{outR} on Pin 8 $SUSM = 20 \log (V_{outL}(20)/V_{outR}(20)) $	20	40	—	dB
Stereo Separation Set-Up Optimized	SUSO	2, 3, 7, 8	Subaddr. 06, Data: 00 Subaddr. 00, Data: 20 Subaddr. 07, Data: n $SUSO = 20 \log (V_{outL}(n)/V_{outR}(20)) $	40	50	—	dB

NOTE: S2 = 2, S3 = ON, S4 = ON. V_{out} is measured on Pins 7 and 8 for K1 and K2, respectively. K1/K2 set-up control may also be used to equalize gains in dual language mode.

DE-EMPHASIS

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Unit
De-Emphasis	DMP	2, 3, 7, 8	$V_p = 50$ mVrms, S1 = ON, S2 = 1, 2 S4 = ON, S5 = ON Subaddr. 06 Data 05, V_{out} measured on Pin 7, 8 $DMP = 20 \log (V_{out}(200 \text{ Hz})/V_{out}(10 \text{ kHz})) $	9.8	10.3*	10.8	dB

* Corresponding to 50 μ s time constant ($\pm 7\%$; 46.5 μ s, 53.5 μ s).

SPECIAL EFFECTS**PSEUDO-STEREO**

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Unit
Frequency for 180° Phase Shift	FREO	5, 17, 18	Subaddr. 06 data 22 Input frequency V_A for phase shift of 180° between V_{out} on Pins 17, 18 re- spectively	1.2	1.25	1.4	kHz
Amplitude	PSA	5, 18	Subaddr. 06 Data 02: V_{outN} Subaddr. 06, Data: 22: V_{outPS} $PSA = 20 \log (V_{outPS}/V_{outN}) $	—	0.1	0.6	dB
	VARI		For frequencies up to 15 kHz			3.0	dB

EXTRA-WIDE (See Notes)

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Unit
Direct Gain Left	LLA	5, 6, 17, 18	$LLA = (V_{outLL} / V_{outNL}) \times 100$	110	120	130	%
Direct Gain Right	RRB	5, 6, 17, 18	$RRB = (V_{outRR} / V_{outNR}) \times 100$	110	120	130	%
Left to Right CC	LRC	5, 6, 17, 18	$LRC = (V_{outNR} \times V_{outLR}) \times 100 / (V_{outNL} \times V_{outRR})$	48	54	60	%
Right to Left CC	RLD	5, 6, 17, 18	$RLD = (V_{outNL} \times V_{outRL}) \times 100 / (V_{outNR} \times V_{outLL})$	48	54	60	%
High Pass Filter	HPLR	5, 6, 17, 18	$HPLR = 20 \log ((V_{outLR} \times V_{300NL}) / (V_{outNL} \times V_{hLR}))$	2.8	3.2	3.6	dB
High Pass Filter	HPRL	5, 6, 17, 18	$HPRL = 20 \log ((V_{outRL} \times V_{300NR}) / (V_{outNR} \times V_{hPRL}))$	2.8	3.2	3.6	dB

NOTES:

Subaddress 06 Data 00

* Fva = 300 Hz

– S2 = 4 output Pin 17: V300NL

– S2 = 5 output Pin 18: V300NR

* Fva = 1 kHz

– S2 = 4 output Pin 17: V_{outNL}– S2 = 5 output Pin 18: V_{outNR}

Subaddress 06 Data 10

* Fva = 300 Hz

– S2 = 4 output Pin 18: VhpLR

– S2 = 5 output Pin 17: VhpRL

* Fva = 1 kHz

– S2 = 4 output Pin 17: V_{outLL}– S2 = 4 output Pin 18: V_{outLR}– S2 = 5 output Pin 17: V_{outRL}– S2 = 5 output Pin 18: V_{outRR}**EXTRA-WIDE AND PSEUDO-STEREO** (See Notes)

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Unit
Left to Right CC	LRBT	5, 6, 17, 18	$LRBT = 100 (V_{spNR} \times V_{spLR}) / (V_{spNL} \times V_{spRR})$	32	37	42	%
Right to Left CC	RLBT	5, 6, 17, 18	$RLBT = 100 (V_{spNN} \times V_{spRL}) / (V_{spNR} \times V_{spLL})$	32	37	42	%

NOTES:

Fva = 1 kHz; Subaddress 06 Data 00

S2 = 4, output on Pin 17: VspNL

S2 = 5, output on Pin 18: VspNR

Subaddress 06 Data 30

S2 = 4, output on Pin 17: VspLL

and output on Pin 18: VspLR

S2 = 5, output on Pin 17: VspRL

and output on Pin 18: VspRR

DISTORTION

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Unit
Distortion	DIST	2, 3	For all selected matrix options. DIST is defined for each output by: $DIST = 100 \times (V_{harm} / V_{tot})$ where V _{tot} is measured on the output corresponding to the selected input (see S2 and the switching matrix table 1) with a low pass filter at 15 kHz and V _{harm} is measured on the same output with a high Q band pass filter from 2 kHz to 15 kHz.	—	0.2	0.5	%
		4					
		5, 6					
		7, 8					
		11, 12					
		15, 16					
17, 18							

* Depending on Matrix Option.

GLITCH

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Unit
Glitch on Outputs When Changing Volume Control	GLU	7, 8, 11, 12, 15, 16, 17, 18	S5 = ON, use a first order RC high pass filter with a frequency cut-off about 10 Hz as per Figure 5. For the first four steps: For the next four steps: For the remaining steps:	— — —	— — —	5 3 1	mVpp
DC Level Change When Changing Matrix Option		7, 8, 11, 12, 15, 16, 17, 18		—	—	100	mV

OTHER PARAMETERS

Characteristics	Symbol	Pin	Test Conditions	Min	Typ	Max	Unit
Analog Ground Polarization (see Note 1)	VAGD	1,13	Vpin28 = VDD = 12 V Vpin14 = Vpin20 = Vpin25 = VSS = 0 V Pin 1 and Pin 13 have to be connected together	5			V
Input Output Polarization (see Note 1)	VPOL	2, 3, 4, 5, 6, 7, 8, 11, 12, 15, 16, 17, 18	Force VAGD = VDD/2 on Pin 1 and Pin 13 and measure VPOL(n) on each input and output pin	5			V
Input and Output Impedance (see Note 1)	IKR IR ORS ORA	2,3 4, 5, 6 7, 8 11, 12 15, 16 17, 18	Force Pin 1 and Pin 13 to VAGD = VDD/2. Force tested pin to VPOL(n) – 0.1 V and measure the source current K(n): IKR(n) = 0.1/K(n) IR(n) = 0.1/K(n) ORS(n) = 0.1/K(n) except for matrix 03 and 0B ORA(n) = 0.1/K(n) ORA(n) = 0.1/K(n) ORA(n) = 0.1/K(n)	25 150 — — — —	— — — — — —	— — 1 200 200 200	kΩ Ω
Noise	NKST NKDM NLMS NOMS NVCT	7, 8, 11, 12, 15, 16 17, 18 17, 18	S5 = ON, Bandwidth 20 Hz – 15 kHz Matrix Option Stereo Input K1 or K2 Matrix Option Dual or Mono or NICAM Stereo, Input K1 or K2 Output LS, Input Mono or SCART Output SCART and Input Mono or Output HiFi/HP and Inputs Mono/SCART Output LS, volctrl step 24 Output HP, volctrl step 12	— — — — —	150 120 90 60 5	— — — — —	μVrms
PSRR Power Supply Rejection	PSRR	15, 16, 17, 18, 28	S6 = ON, Vout measured on each output PSRR = 20 log (Vout/Vr) For LS Outputs For Other Outputs	— —10 —30	— —12 —40	— — —	dB

NOTES:

1. This test measurement is done directly on the device without any external wiring and hardware, excepting short circuit between Pins 1 and 13.
2. Output drive capability when using application circuit is 1 Vpp on 10 kΩ for all outputs.

SWITCHING MATRIX TABLE

Selection Code bcdefgh	HEXA Code 3)	Input					Ident Code	Output						Notes
		MONO	K1	K2	SCART			LS		HP		SCART		
					L	R	L	R	L	R	L	R		
STEREO TRANSMISSION														
0XX0100	04	—			—	—	01	L	R	L	R	L	R	
0XX0011	03	—			—	—	01	L	R	L	R	M*	M*	1
0XX0000	00	—			L°	R°	01	L°	R°	L°	R°	L	R	
1XX0000	40	—	(L+R)/2	R	1°	2°	01	1°	1°	1°	1°	L	R	
0XX0010	02	—			1°	2°	01	1°	1°	2°	2°	L	R	
0XX0001	01	—			1°	2°	01	2°	2°	1°	1°	L	R	
1XX0001	41	—			1°	2°	01	2°	2°	2°	2°	L	R	
DUAL LANGUAGE OR MONO TRANSMISSION														
1XX0100	44	—	1	2	—	—	10	1	1	1	1	1	2	
0XX0110	06	—	1	2	—	—	10	1	1	2	2	1	2	
0XX0101	05	—	1	2	—	—	10	2	2	1	1	1	2	
1XX0101	45	—	1	2	—	—	10	2	2	2	2	1	2	
0XX1111	0F	—	1	—	—	—	00	1	1	1	1	1	1	2
0XX0111	07	—	1	2	—	—	10	2	2	2	2	2	2	
0XX1011	0B	—	1	2	—	—	10	2	2	1	1	2	2	
0XX1000	08	—	1	2	L°	R°	10	L°	R°	L°	R°	1	2	
0XX1100	0C	—	1	—	L°	R°	00	L°	R°	L°	R°	1	1	2
1XX1011	4B	—	1	2	L°	R°	00	L°	R°	L°	R°	2	2	
1XX0110	46	—	1	2	1°	2°	10	1°	1°	1°	1°	1	2	
0XX1010	0A	—	1	2	1°	2°	10	1°	1°	2°	2°	1	2	
0XX1001	09	—	1	2	1°	2°	10	2°	2°	1°	1°	1	2	
1XX0111	47	—	1	2	1°	2°	10	2°	2°	2°	2°	1	2	
1XX0010	42	—	1	—	1°	2°	00	1°	1°	1°	1°	1	1	2
0XX1110	0E	—	1	—	1°	2°	00	1°	1°	2°	2°	1	1	2
0XX1101	0D	—	1	—	1°	2°	00	2°	2°	1°	1°	1	1	2
1XX0011	43	—	1	—	1°	2°	00	2°	2°	2°	2°	1	1	2
AM TRANSMISSION														
1XX1100	4C	AM	—	—	L°	R°	—	L°	R°	L°	R°	AM	AM	
1XX1000	48	AM	—	—	1°	2°	—	1°	1°	1°	1°	AM	AM	
1XX1110	4E	AM	—	—	1°	2°	—	1°	1°	2°	2°	AM	AM	
1XX1101	4D	AM	—	—	1°	2°	—	2°	2°	1°	1°	AM	AM	
1XX1001	49	AM	—	—	1°	2°	—	2°	2°	2°	2°	AM	AM	
1XX1111	4F	AM	—	—	—	—	—	AM	AM	AM	AM	AM	AM	

NOTES:

- M* is the de-emphasized signal of K1, generated in this way:
(L+R)/2 and R → L & R → De-emphasis → (L+R)/2 = M*
- Input K1 may be first language or mono information (indent code 10 or 00).
- With c = d = 0.

REMARKS:

- To output HIFI the same input is fed as to output LS.
- HEXA Code 4A is not used.
- HEXA Codes 00 – 0F and 4C – 4F excepting 07 are compatible with respective codes on earlier versions.

LOUDSPEAKER OUTPUT

TONE CONTROL

Treble and bass are controlled in 14 steps from minimum to maximum using a 4-bit word for each. Signal alternations are identical on both channels and are realized by variable switched capacitor filters providing very low dispersion characteristics.

In order to prevent clipping of the signal if input amplitude is high and tone control boosts it to values approaching supply voltages, two auxiliary attenuators have been placed on the front end of the tone control circuit, one for the left channel and one for the right.

These attenuators are switched on only if bass boost might generate distortion, i.e., if one of the four highest levels for bass enhancement is selected (steps 11 to 14).

To compensate occurring signal attenuation, volume control on LS output may then be shifted correspondingly to higher levels by means of software control.

Figure 2 shows how the circuit works for one channel.

As a result, up to bass control step 10 (including flat response condition), auxiliary attenuator is disabled. When one of the four last steps is addressed, signal amplitude on the input of the tone control circuit will be reduced (by 2.5/5/7.5 or 10 dB for steps 11, 12, 13, or 14, respectively). On the output, signal loss will only be perceptible if volume control cannot be shifted anymore to sufficiently high values because maximum level is reached. This limitation, however, may avoid generation of amplitudes saturating output amplifiers.

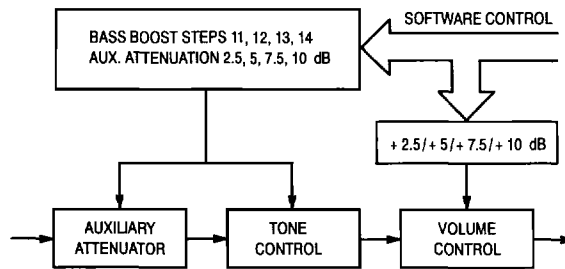


Figure 2.

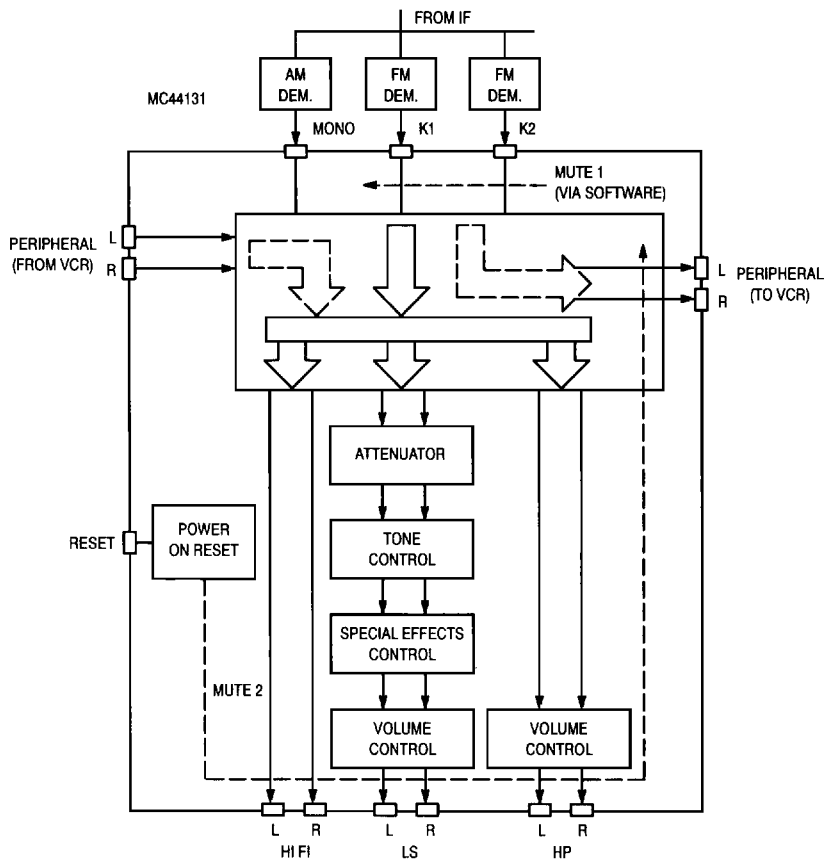


Figure 3. Input/Output Combinations

EMI SUPPRESSION

When using ICs in or near television receiver circuits, EMI (electromagnetic interference) and subsequent unwanted display artifacts and distortion are probable unless adequate EMI suppression is implemented. A common misconception is that some offending digital device is the culprit. This is erroneous in that an IC itself has insufficient surface area to produce sufficient radiation. The device, while it is the generator of interfering signals, must be coupled to an antenna before EMI is radiated. The source for the EMI is not the IC which generates the offending signals but rather the circuitry which is attached to the IC.

Potential EMI signals are generated by *all* digital devices. Whether they become a nuisance is dependent upon their frequency and whether they have a sufficient antenna. The frequency and number of these signals is affected by both circuit design within the IC and the manufacturing process. Device speed is also a major contributor of potential EMI. Because the design is determined by the anticipated application, the manufacturing process is fixed and the drive for speed ever increasing, the only effective point to implement EMI suppression is in the PC board design. The PC board usually is the antenna which radiates the EMI. The most efficient method of minimizing EMI radiation is to minimize the efficiency of this antenna.

The most common cause of inadequate EMI suppression lies with the ground system of the suspected digital devices. As pointed out previously, di/dt transitions can be significant in digital circuits. If the di/dt transitions appear in the ground system and the ground system is inductive, the harmonics present in these transitions are a source of potential EMI signals. The unfortunate result of putting digital devices on a reactive ground system is guaranteed EMI problems.

The area which should be addressed first as a potential EMI source is the ground. Without an adequate ground system, EMI cannot be effectively reduced by decoupling. If at all possible, the ground should be a complete unbroken plane. Figure 4 shows two examples of relieving ground around device pins. When relieving vias and plated through holes, large areas of ground loss should be avoided. When the relief pattern is equal to half the distance between pins, over etching and process errors may remove ground between pins. If sufficient ground around enough pins are removed, the ground system can become isolated or nearly isolated "patches" which will appear inductive. If ground, such as the vicinity of an IC, must be removed, replace with a cross hatch of ground lines with the mesh as small as possible.

If a single unbroken plane can be devoted to the ground system, EMI can usually be sufficiently suppressed by using ferrite beads on suspect EMI paths and decoupling with ade-

quate values of capacitors. The value of the decoupling capacitor depends on the frequency and amplitude of the offending signals. Ferrite beads are available in a wide variety of shape, size and material to fit virtually any application.

Choose a ferrite bead for desired impedance at the desired frequency and construct a low pass filter using one or more appropriate capacitors in a "L", "T" or "PI" arrangement. Use only capacitors of low inductive and resistive properties such as ceramic or mica. Install filters in series with each IC pin suspected of contributing offending EMI signals and as close to the pin as possible. Analysis using a spectrum analyzer can help determine which pins are suspect.

Where PC board costs constrain the number of layers available, and if the EMI frequencies are far removed from the frequencies of operation, ferrite beads and decoupling capacitors may still be effective in reducing EMI emissions. Where only two (or in some cases, only one!) layer is used, the ground system is always reactive and poses an EMI problem. If the offending EMI and normal operating frequency differ sufficiently, filtering can still work.

An "island" is constructed in the ground system for the digital device using ferrite beads and decoupling capacitors as shown by the example in Figure 5. The ground must be cut so that the digital ground for the device is isolated from the rest of the ground system. Next choose a ferrite bead of the appropriate value. Install this bead between the isolated ground and the ground system. Install low pass filters in all suspect lines with the capacitor closest to the device pin connected to the isolated ground in all signal lines where EMI is suspect. Also cut the power to the device and insert a ferrite bead as shown in Figure 5. Finally, decouple the device between the power pin(s) and isolated ground pin(s) using a low inductive/resistive capacitor of adequate value.

The methods described above will work acceptably when the EMI frequency and the frequency of operation of the device generating the EMI differ greatly. Where the EMI is disturbing the high VHF or UHF channels and the device generating the EMI is operating within the NTSC/PAL bandwidth, the energy contained in the harmonics generating the EMI is situated well above the operating frequency and suppressing this type of EMI poses no great problem. However, if the EMI is present on low VHF channels and/or the operation of the device is outside the NTSC/PAL bandwidth, such as a 2X pixel clock or 4x fsc oscillator, compromise between video quality and suppression complexity is usually required to obtain an acceptable solution. For those cases where the operating frequency of the device is very near the frequency of the EMI disturbance, careful attention to PCB layout, multiple layer PCB and even shielding may be necessary to obtain an acceptable design.

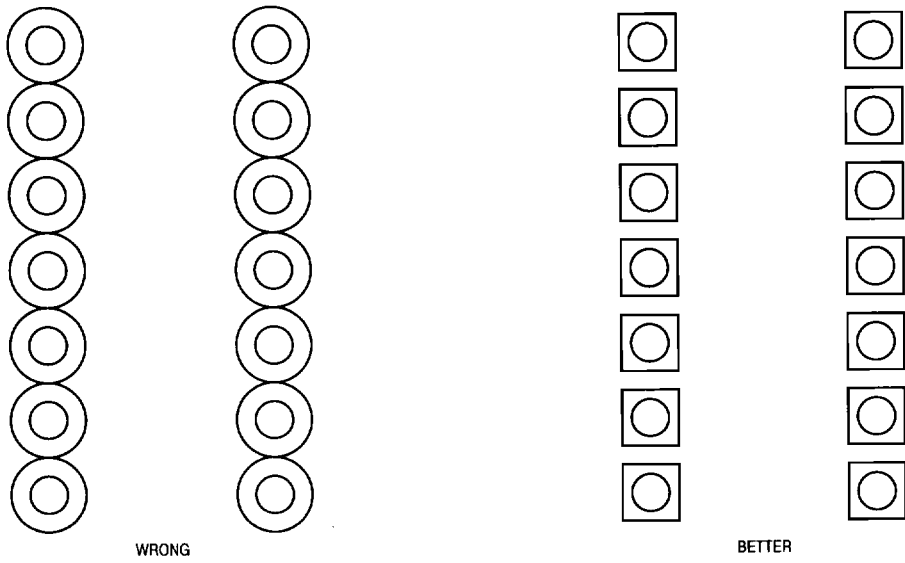


Figure 4.

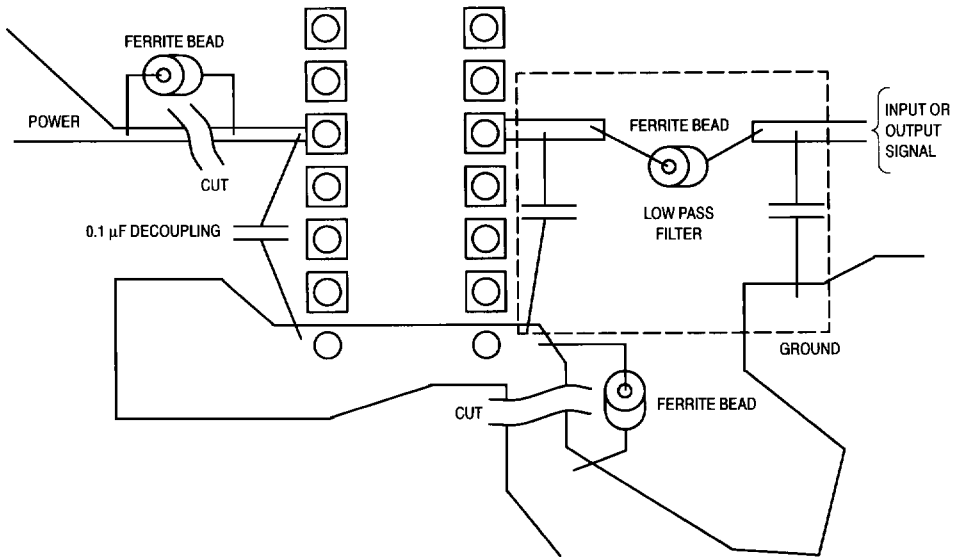


Figure 5.