

**SN54HCT651, SN54HCT652, SN74HCT651, SN74HCT652  
OCTAL BUS TRANSCEIVERS AND REGISTERS  
WITH 3-STATE OUTPUTS**

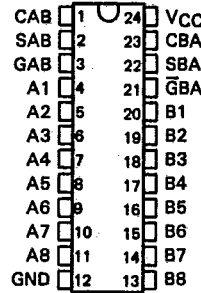
D2804, MARCH 1984—REVISED SEPTEMBER 1987

- Inputs are TTL-Voltage Compatible
- Bus Transceivers and Registers
- Independent Registers and Enables for A and B Buses
- High-Current 3-State Outputs Can Drive Up to 15 LSTTL Loads
- Multiplexed Real-Time and Stored Data
- Choice of True and Inverting Data Paths
- Package Options Include Plastic "Small Outline" Packages, Ceramic Chip Carriers, and Standard Plastic and Ceramic 300-mil DIPs
- Dependable Texas Instruments Quality and Reliability

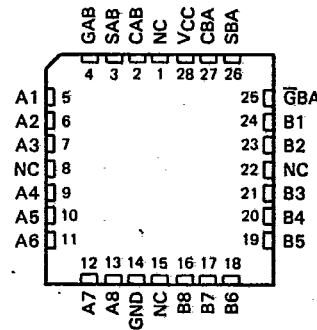
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**HCMOS Devices**

SN54HCT651, SN54HCT652 ... JT PACKAGE  
SN74HCT651, SN74HCT652 ... DW OR NT PACKAGE  
(TOP VIEW)



SN54HCT651, SN54HCT652 ... FK PACKAGE  
(TOP VIEW)



NC—No internal connection

**description**

These devices consist of bus transceiver circuits, D-type flip-flops, and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Enable GAB and  $\overline{GBA}$  are provided to control the transceiver functions. SAB and SBA control pins are provided to select whether real-time or stored data is transferred. A low input level selects real-time data, and a high selects stored data. The examples on the following page demonstrate the four fundamental bus-management functions that can be performed with the 'HCT651 and 'HCT652.

Data on the A or B data bus, or both, can be stored in the internal D flip-flops by low-to-high transitions at the appropriate clock pins (CAB or CBA) regardless of the select or enable control pins. When SAB and SBA are in the real-time transfer mode, it is also possible to store data without using the internal D-type flip-flops by simultaneously enabling GAB and  $\overline{GBA}$ . In this configuration each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines will remain at its last state.

The SN54HCT651 and SN54HCT652 are characterized for operation over the full military temperature range of -55°C to 125°C. The SN74HCT651 and SN74HCT652 are characterized for operation from -40°C to 85°C.

PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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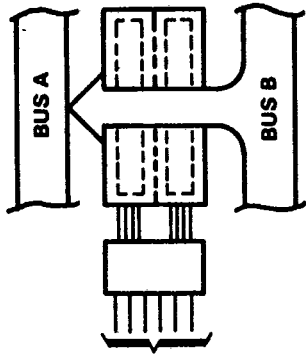
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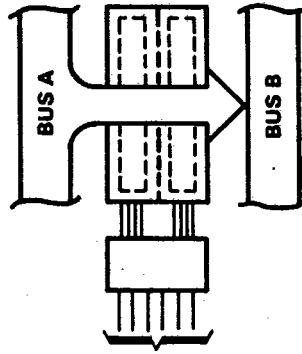
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**HCMOS Devices**



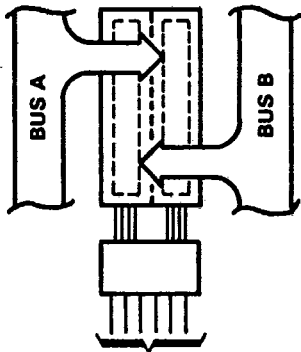
(3)	(21)	(1)	(23)	(2)	(22)
GAB	$\bar{G}BA$	CAB	CBA	SAB	SBA
L	L	X	X	X	L

**REAL-TIME TRANSFER**  
**BUS B TO BUS A**



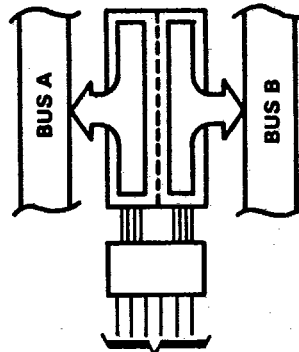
(3)	(21)	(1)	(23)	(2)	(22)
GAB	$\bar{G}BA$	CAB	CBA	SAB	SBA
H	H	X	X	L	X

**REAL-TIME TRANSFER**  
**BUS A TO BUS B**



(3)	(21)	(1)	(23)	(2)	(22)
GAB	$\bar{G}BA$	CAB	CBA	SAB	SBA
X	H	↑	X	X	X
L	X	X	↑	X	X
L	H	↑	↑	X	X

**STORAGE FROM**  
**A AND/OR B**



(3)	(21)	(1)	(23)	(2)	(22)
GAB	$\bar{G}BA$	CAB	CBA	SAB	SBA
H	L	H or L	H or L	H	H

**TRANSFER**  
**STORED DATA**  
**TO A AND/OR B**

Pin numbers shown are for DW, JT, and NT packages.

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FUNCTION TABLE

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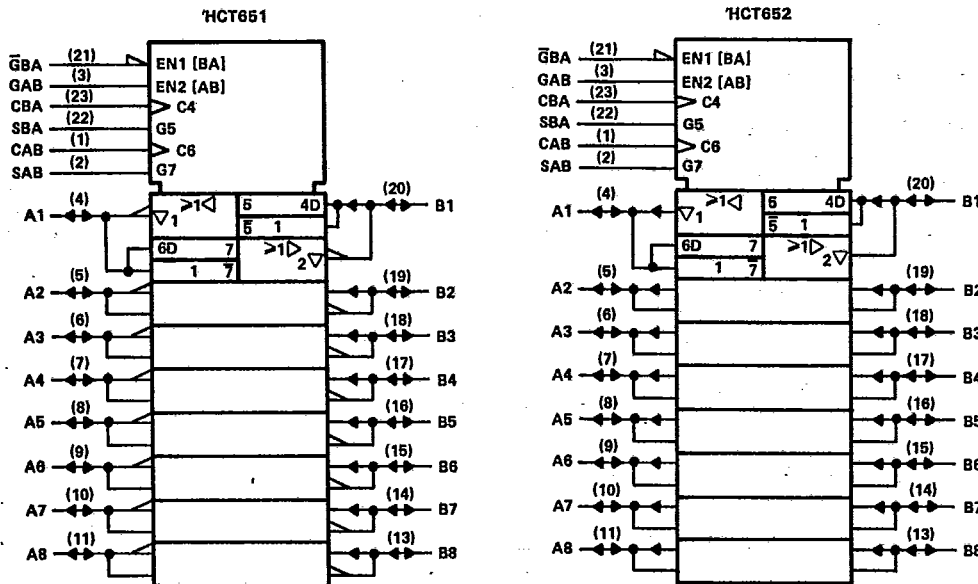
INPUTS						DATA I/O†		OPERATION OR FUNCTION	
GAB	G̅BA	CAB	CBA	SAB	SBA	A1 THRU A8	B1 THRU B8	HCT651	HCT652
L	H	H or L	H or L	X	X	Input	Input	Isolation	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B Data	Store A and B Data
X	H	↑	H or L	X	X	Input	Not specified	Store A, Hold B	Store A, Hold B
H	H	↑	↑	X	X	Input	Output	Store A in both registers	Store A in both registers
L	X	H or L	↑	X	X	Not specified	Input	Hold A, Store B	Hold A, Store B
L	L	↑	↑	X	X	Output	Input	Store B in both registers	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-Time B̅ Data to A Bus	Real-Time B Data to A Bus
L	L	X	H or L	X	H	Output	Input	Stored B̅ Data to A Bus	Stored B Data to A Bus
H	H	X	X	L	X	Input	Output	Real-Time A̅ Data to B Bus	Real-Time A Data to B Bus
H	H	H or L	X	H	X	Input	Output	Stored A̅ Data to B Bus	Stored A Data to B Bus
H	L	H or L	H or L	H	H	Output	Output	Stored A̅ Data to B Bus and Stored B̅ Data to A Bus	Stored A Data to B Bus and Stored B Data to A Bus

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HCMOS Devices

†The data output functions may be enabled or disabled by various signals at the GAB and G̅BA inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

logic symbols‡



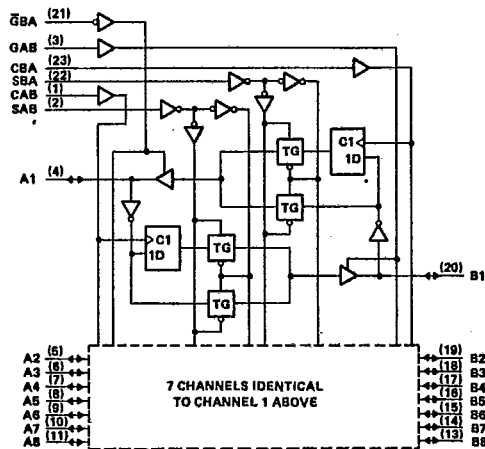
‡These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12. Pin numbers shown are for DW, JT, and NT packages.

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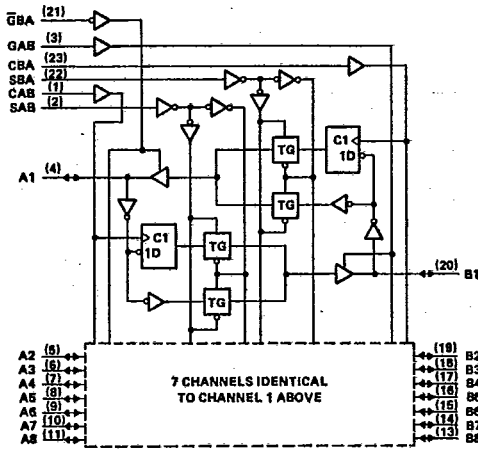
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logic diagrams (positive logic)

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Pin numbers shown are for DW, JT, and NT packages.

**absolute maximum ratings over operating free-air temperature†**

Supply voltage, $V_{CC}$ .....	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) .....	$\pm 20$ mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) .....	$\pm 20$ mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ ) .....	$\pm 35$ mA
Continuous current through $V_{CC}$ or GND pins .....	$\pm 70$ mA
Lead temperature 1,6 mm (1/16 in) from case for 60 s: FK or JT package .....	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 s: DW or NT package .....	260°C
Storage temperature range .....	-65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

**recommended operating conditions**

	SN54HCT651			SN74HCT651			UNIT
	SN54HCT652			SN74HCT652			
	MIN	NOM	MAX	MIN	NOM	MAX	
$V_{CC}$ Supply voltage	4.5	5	5.5	4.5	5	5.5	V
$V_{IH}$ High-level input voltage	$V_{CC} = 4.5$ V to $5.5$ V			2			V
$V_{IL}$ Low-level input voltage	$V_{CC} = 4.5$ V to $5.5$ V			0			V
$V_I$ Input voltage	0	$V_{CC}$		0	$V_{CC}$		V
$V_O$ Output voltage	0	$V_{CC}$		0	$V_{CC}$		V
$t_t$ Input transition (rise and fall) times	0	500		0	500		ns
$T_A$ Operating free-air temperature	-65	125		-40	85		°C

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HCT651 SN54HCT652		SN74HCT651 SN74HCT652		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OH</sub> = -20 μA	4.5 V	4.4	4.499		4.4		4.4	V	
	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OH</sub> = -6 mA	4.5 V	3.98	4.30		3.7		3.84		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OL</sub> = 20 μA	4.5 V		0.001	0.1		0.1	0.1	V	
	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> , I <sub>OL</sub> = 6 mA	4.5 V		0.17	0.26		0.4	0.33		
I <sub>I</sub>	Control Inputs V <sub>I</sub> = V <sub>CC</sub> or 0	5.5 V		±0.1	±100		±1000	±1000	nA	
I <sub>OZ</sub>	A or B V <sub>O</sub> = V <sub>CC</sub> or 0, V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> Data = V <sub>CC</sub> or 0	5.5 V		±0.01	±0.5		±10	±5	μA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0	5.5 V			8		160	80	μA	
ΔI <sub>CC</sub> †	One input at 0.5 V or 2.4 V Other inputs at 0 V or V <sub>CC</sub>	5.5 V		1.4	2.4		3	2.9	mA	
C <sub>I</sub>	Control Inputs	4.5 to		3	10		10	10	pF	
		5.5 V								

†This is the increase in supply current for each input that is at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

timing requirements over recommended operating free-air temperature range (unless otherwise noted)

	V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HCT651 SN54HCT652		SN74HCT651 SN74HCT652		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub> Clock frequency	4.5 V	0	25	0	17	0	20	MHz
	5.5 V	0	28	0	19	0	22	
t <sub>w</sub> Pulse duration, CBA or CAB high or low	4.5 V		20		30		25	ns
	5.5 V		18		27		23	
t <sub>su</sub> Setup time, A before CBA1 or B before CBA†	4.5 V		15		23		19	ns
	5.5 V		14		21		17	
t <sub>h</sub> Hold time, A after CBA1 or B after CBA†	4.5 V		5		5		5	ns
	5.5 V		5		5		5	

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted),  $C_L = 50$  pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HCT651 SN54HCT652		SN74HCT651 SN74HCT652		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			4.5 V 5.5 V	25 28	35 40		17 19	20 22		MHz	
t <sub>pd</sub>	CBA or CAB	A or B	4.5 V 5.5 V		18 16	36 32	54 49	45 41		ns	
t <sub>pd</sub>	A or B	B or A	4.5 V 5.5 V		14 12	27 24	41 37	34 31		ns	
t <sub>pd</sub>	SBA or SAB†	A or B	4.5 V 5.5 V		20 17	38 34	57 51	48 43		ns	
t <sub>en</sub>	$\bar{C}$ BA or GAB	A or B	4.5 V 5.5 V		25 22	49 44	74 67	61 55		ns	
t <sub>dis</sub>	$\bar{C}$ BA or GAB	A or B	4.5 V 5.5 V		25 22	49 44	74 67	61 55		ns	
t <sub>t</sub>		Any	4.5 V 5.5 V		9 7	12 11	18 16	15 14		ns	

C <sub>pd</sub>	Power dissipation capacitance	No load, T <sub>A</sub> = 25°C	50 pF typ
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switching characteristics over recommended operating free-air temperature range (unless otherwise noted),  $C_L = 150$  pF (see Note 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HCT651 SN54HCT652		SN74HCT651 SN74HCT652		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t <sub>pd</sub>	CBA or CAB	A or B	4.5 V 5.5 V		24 22	53 47	80 72	66 60		ns	
t <sub>pd</sub>	A or B	B or A	4.5 V 5.5 V		22 20	44 39	70 60	55 50		ns	
t <sub>pd</sub>	SBA or SAB†	A or B	4.5 V 5.5 V		26 24	55 49	83 74	69 62		ns	
t <sub>en</sub>	$\bar{C}$ BA or GAB	A or B	4.5 V 5.5 V		33 30	66 59	100 90	82 74		ns	
t <sub>t</sub>		Any	4.5 V 5.5 V		17 14	42 38	63 57	53 48		ns	

NOTE 1: Load circuits and voltage waveforms are shown in Section 1.

†These parameters are measured with the internal output state of the storage register opposite to that of the bus input.

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