

Silicon diffused power transistors

BUW11; BUW11A

High-voltage, high-speed, glass-passivated npn power transistors in a SOT93 envelope, intended for use in converters, inverters, switching regulators, motor control systems etc.

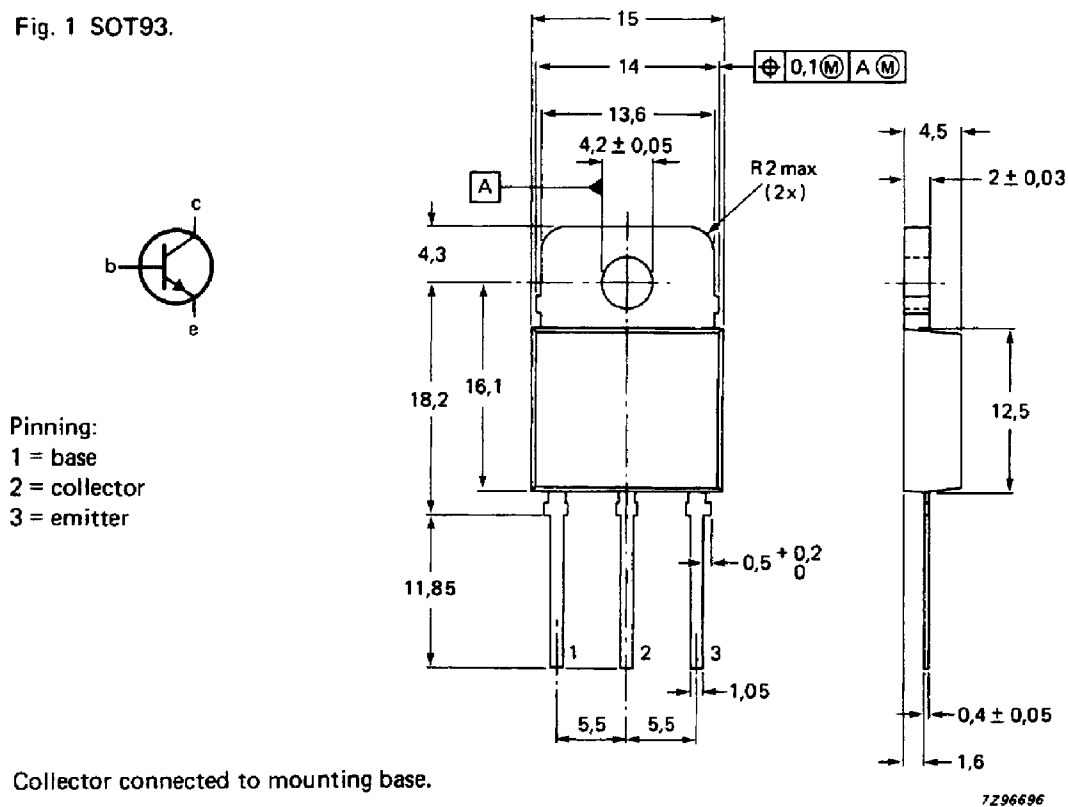
QUICK REFERENCE DATA

		BUW11	BUW11A	
Collector-emitter voltage (peak value; $V_{BE} = 0$)	V_{CESM} max.	850	1000	V
Collector-emitter voltage (open base)	V_{CEO} max.	400	450	V
Collector-emitter saturation voltage	V_{CESat} max.	1.5		V
Collector current (DC)	I_C max.	5		A
Collector current (peak value)	I_{CM} max.	10		A
Total power dissipation up to $T_{mb} = 25^\circ C$	P_{tot} max.	100		W
Fall time (resistive load)	t_f max.	0.8		μs

MECHANICAL DATA

Dimensions in mm

Fig. 1 SOT93.



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RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)

			BUW11	BUW11A	
Collector-emitter voltage (peak value; $V_{BE} = 0$)	V_{CESM}	max.	850	1000	V
Collector-emitter voltage (open base)	V_{CEO}	max.	400	450	V
Collector current (DC)	I_C	max.	5		A
Collector current (peak value) $t_p < 2$ ms	I_{CM}	max.	10		A
Base current (DC)	I_B	max.	2		A
Base current (peak value); $t_p < 2$ ms	I_{BM}	max.	4		A
Total power dissipation up to $T_{mb} = 25$ °C	P_{tot}	max.	100		W
Storage temperature range	T_{stg}		-65 to +150		°C
Junction temperature	T_j	max.	150		°C

THERMAL RESISTANCE

From junction to mounting base	$R_{th\ j-mb}$	=	1,25		K/W
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CHARACTERISTICS

 $T_j = 25$ °C unless otherwise specified

Collector cut-off current*

 $V_{CE} = V_{CESMmax}; V_{BE} = 0$ $V_{CE} = V_{CESMmax}; V_{BE} = 0; T_j = 125$ °C

I_{CES}	max.	1		mA
I_{CES}	max.	2		mA

Emitter cut-off current

 $I_C = 0; V_{EB} = 9$ V

I_{EBO}	max.	10		mA
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Saturation voltages

 $I_C = 3$ A; $I_B = 0,6$ A $I_C = 2,5$ A; $I_B = 0,5$ A

			BUW11	BUW11A	
V_{CEsat}	max.	1,5	-		V
V_{BEsat}	max.	1,4	-		V
V_{CEsat}	max.	-	1,5		V
V_{BEsat}	max.	-	1,4		V

Collector-emitter sustaining voltage

 $I_C = 100$ mA; $I_{Boff} = 0$; $L = 25$ mH

$V_{CEO_{sust}}$	min.	400	450		V
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Collector saturation current

 $V_{CE} = 1,5$ V

I_{Csat}	max.	3	2,5		A
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DC current gain

 $I_C = 5$ mA; $V_{CE} = 5$ V

h_{FE}	min.	10		
h_{FE}	typ.	18		
h_{FE}	max.	35		

 $I_C = 500$ mA; $V_{CE} = 5$ V

h_{FE}	min.	10		
h_{FE}	typ.	20		
h_{FE}	max.	35		

* Measured with a half sinewave voltage (curve tracer).



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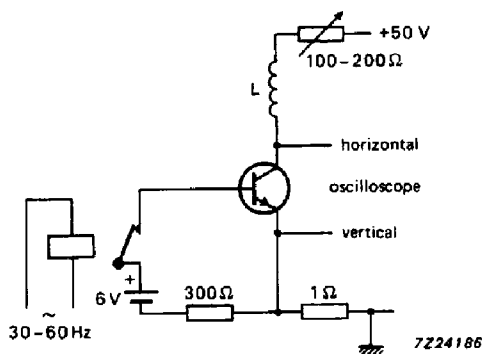


Fig. 2 Test circuit for $V_{CE0sust}$.

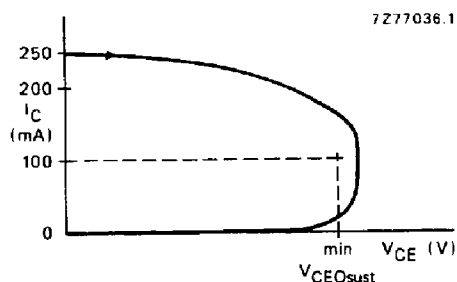


Fig. 3 Oscilloscope display for sustaining voltage.

Switching times resistive load (Figs 4 and 5)

$I_{Con} = 3\text{ A}; I_{Bon} = I_{Boff} = 0,6\text{ A}$

Turn-on time

Turn-off: Storage time

Fall time

$I_{Con} = 2,5\text{ A}; I_{Bon} = -I_{Boff} = 0,5\text{ A}$

Turn-on time

Turn-off: Storage time

Fall time

Switching times inductive load (Figs 6 and 7)

$I_{Con} = 3\text{ A}; I_B = 0,6\text{ A}$

Turn-off: Storage time

Fall time

$I_{Con} = 3\text{ A}; I_B = 0,6\text{ A}; T_j = 100\text{ }^\circ\text{C}$

Turn-off: Storage time

Fall time

Switching times inductive load (Figs 6 and 7)

$I_{Con} = 2,5\text{ A}; I_B = 0,5\text{ A}$

Turn-off: Storage time

Fall time

$I_{Con} = 2,5\text{ A}; I_B = 0,5\text{ A}; T_j = 100\text{ }^\circ\text{C}$

Turn-off: Storage time

Fall time

		BUW11	BUW11A	
t_{on}	max.	1	—	μs
t_s	max.	4	—	μs
t_f	max.	0,8	—	μs
t_{on}	max.	—	1	μs
t_s	max.	—	4	μs
t_f	max.	—	0,8	μs
t_s	typ.	1,1	—	μs
	max.	1,4	—	μs
t_f	typ.	80	—	ns
	max.	150	—	ns
t_s	typ.	1,2	—	μs
	max.	1,5	—	μs
t_f	typ.	140	—	ns
	max.	300	—	ns
t_s	typ.	—	1,1	μs
	max.	—	1,4	μs
t_f	typ.	—	80	ns
	max.	—	150	ns
t_s	typ.	—	1,2	μs
	max.	—	1,5	μs
	typ.	—	140	ns
	max.	—	300	ns

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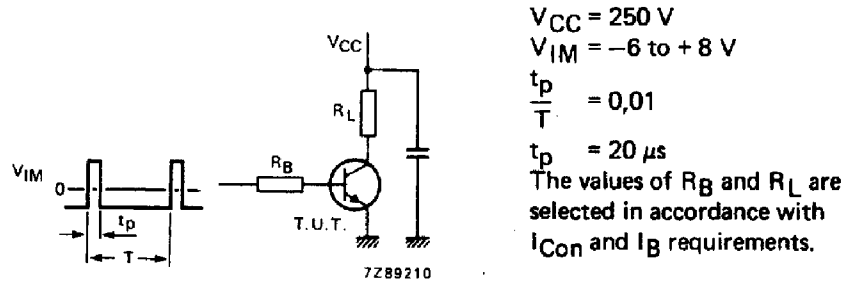


Fig. 4 Test circuit resistive load.

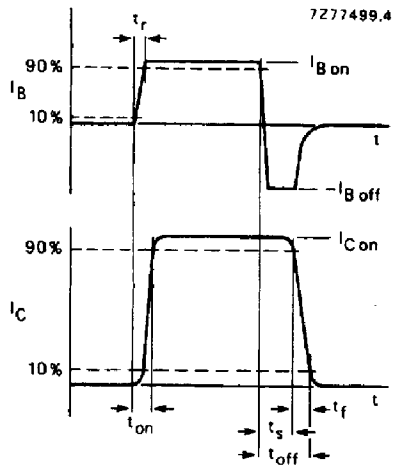


Fig. 5 Switching times waveforms with resistive load.

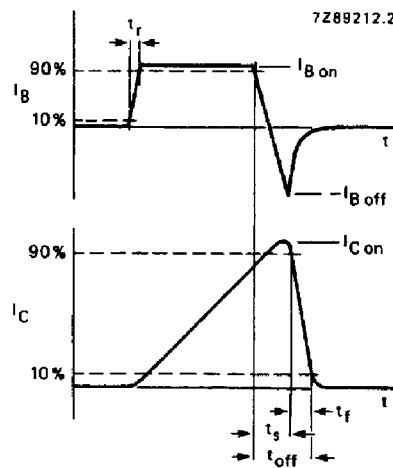


Fig. 6 Switching times waveforms with inductive load.

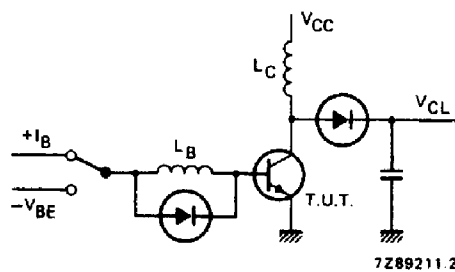


Fig. 7 Test circuit inductive load.

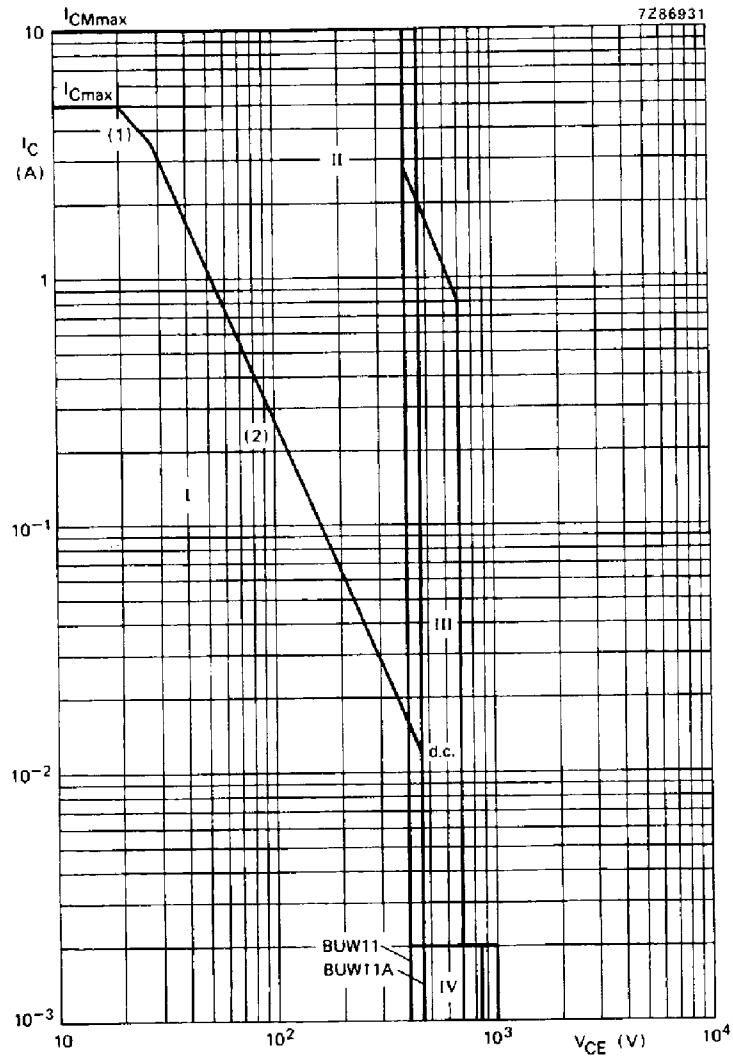
$V_{CL} = 300 \text{ V}$
 $V_{CC} = 30 \text{ V}$
 $-V_{BE} = 5 \text{ V}$
 $L_B = 1 \mu\text{H}$
 $L_C = 200 \mu\text{H}$

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- (1) P_{tot} max line.
- (2) Second-breakdown limits.
- I Region of permissible DC operation
- II Permissible extension for repetitive pulse operation
- III Area of permissible operation during turn-on in single transistor converters, provided $R_{BE} \leq 100 \Omega$ and $t_p \leq 0,6 \mu s$.
- IV Repetitive pulse operation in this region is permissible provided $V_{BE} \leq 0$ and $t_p \leq 5 ms$.

Fig. 8 Safe operating area at $T_{mb} \leq 25^\circ C$.

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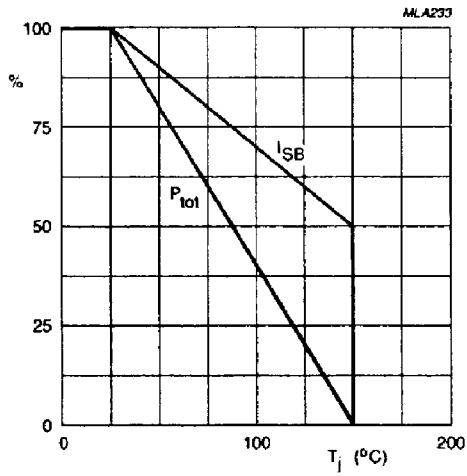


Fig. 9 Total power dissipation derating curve.

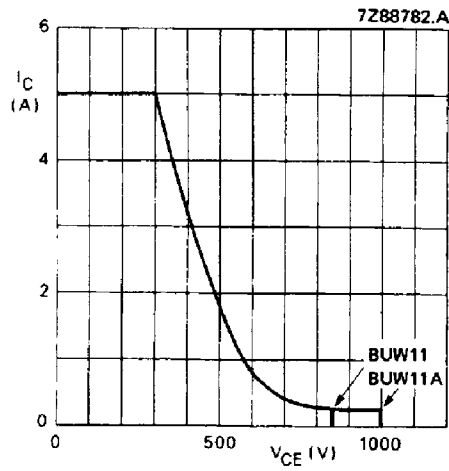


Fig. 10 Reverse bias SOAR.

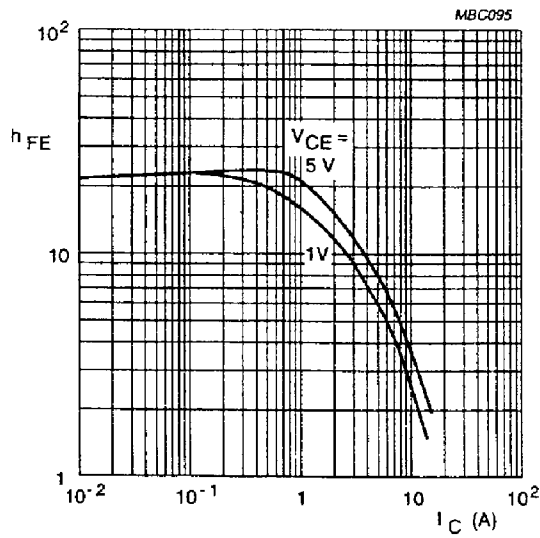


Fig.11 Typical values DC current gain.

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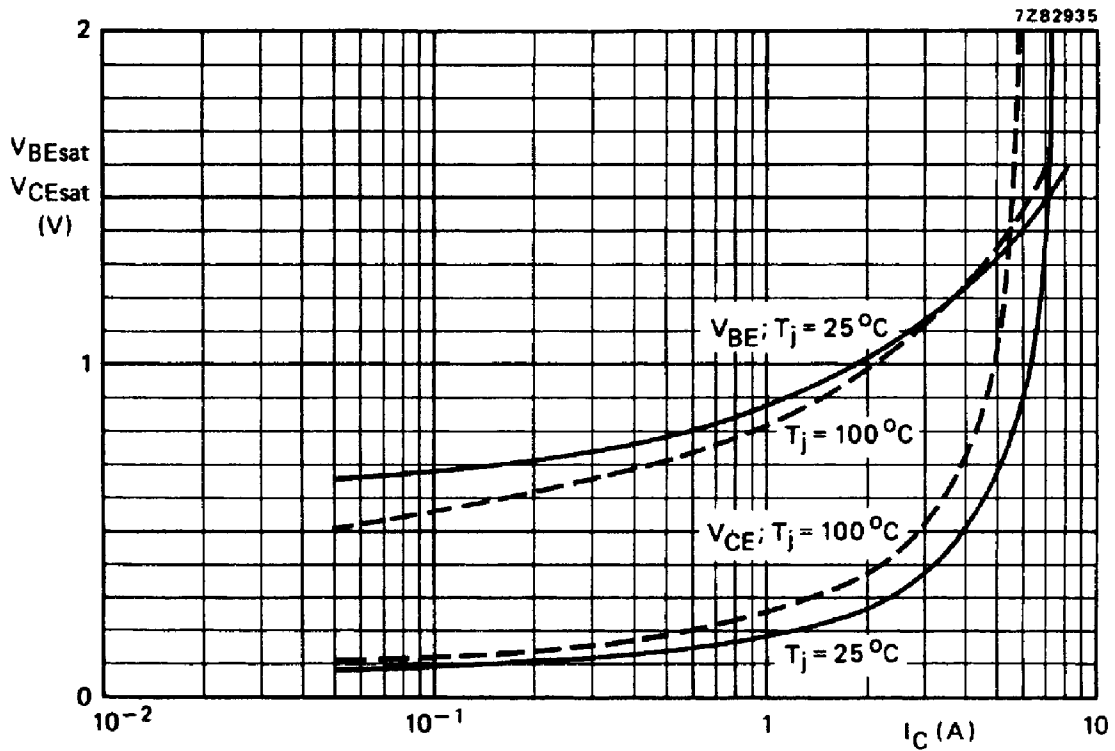


Fig. 12 Typical values base-emitter and collector-emitter voltage, $I_C/I_B = 5$.

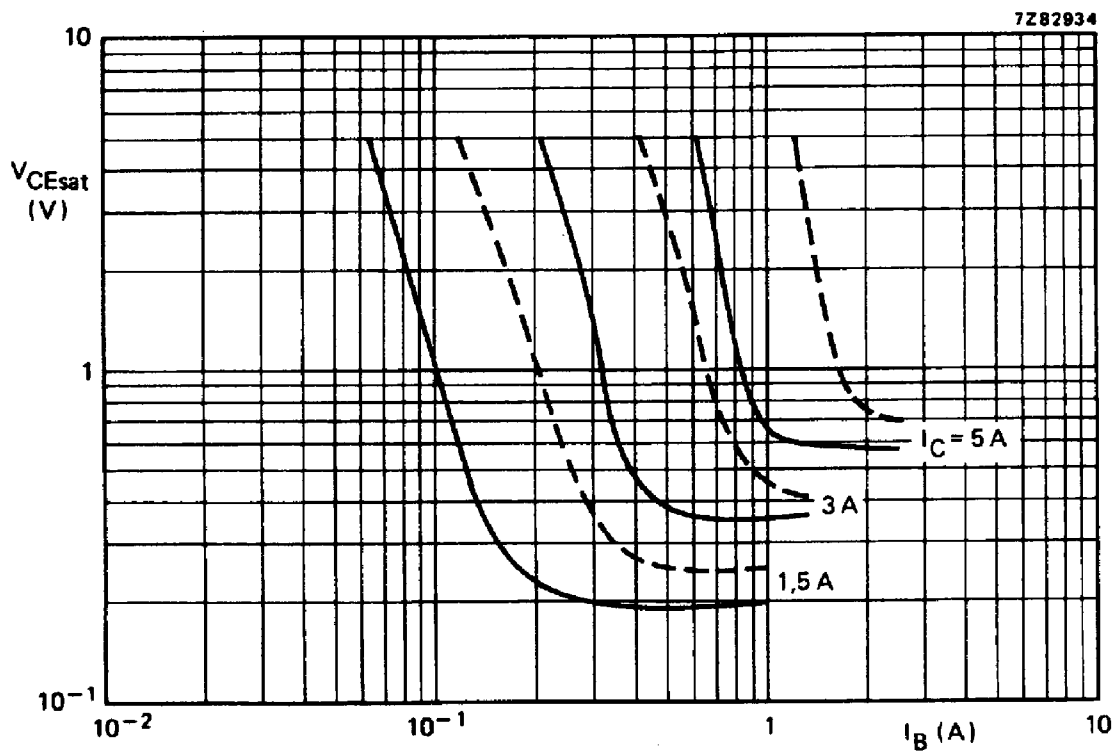


Fig. 13 Typ. (—) and max. (---) values collector-emitter saturation voltage at $T_j = 25^\circ\text{C}$.

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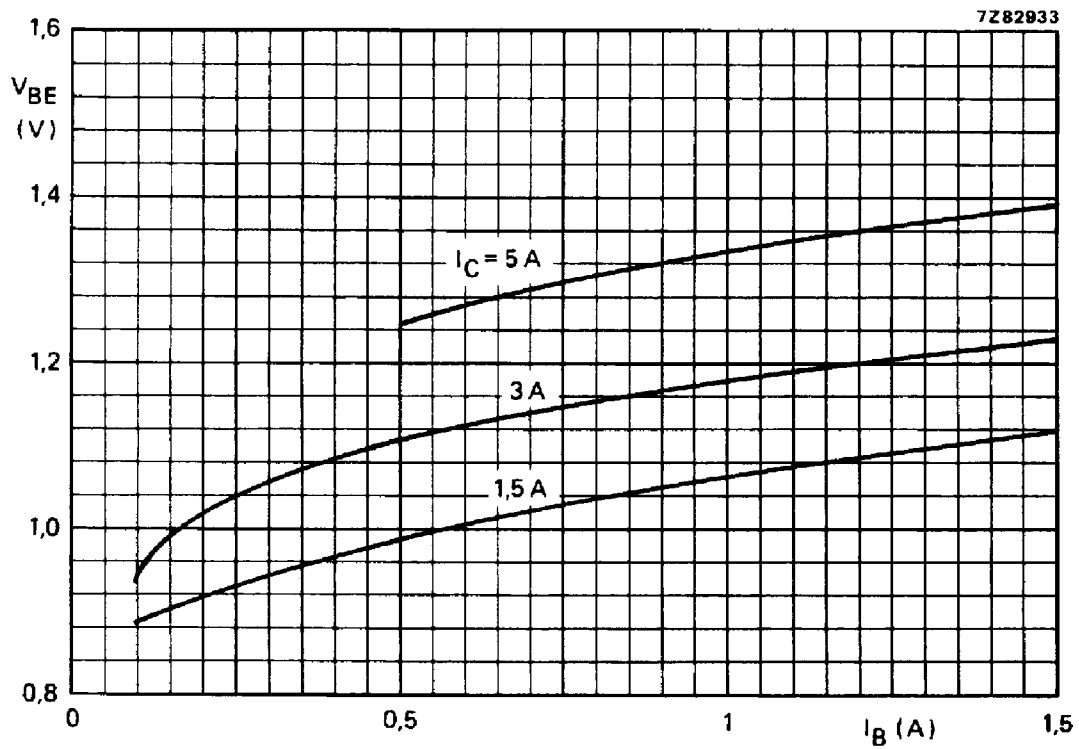


Fig. 14 Typical values at $T_j = 25^\circ\text{C}$.

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