o HIGH SPEED PLL WITH BUILT-IN PRESCALER

The TC9171P/72P/82P-1 are hige-speed PLL-LSI developed for digital tuning system use, and contain 2-modulus prescaler.

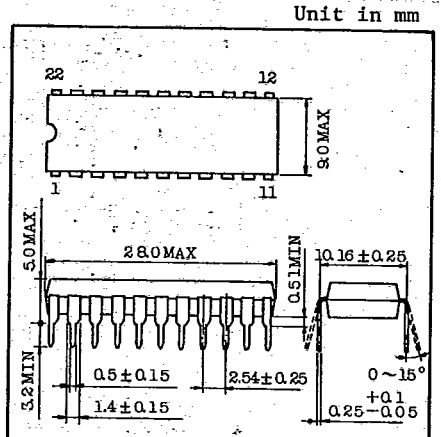
When they are used in combination with system controller LSI TC9301AN/02AF/03AN series, high performance digital synthesized tuner can be realized.

- They contain prescaler, and can directly input the frequency signal of 120 MHz max. at FM band.
- Either pulse swallow dividing type or direct dividing type can be applied depending upon receiving band.
- Both high function type (DIP 22 pin) and conventional type (DIP 16 pin) are provided. High function type contains IF counter which counts IF signal at FM/AM band each and produces auto-stop signal
- Reference frequency is supplied from the controller LSI, and no crystal oscillator is required on the PLL LSI.
- They have two phase comparator outputs, and can use two kinds of low pass filters without changing.
- Abundant general pourpose input-output terminals make possible the control of radio frequency circuit part.
- Frequency input terminals are provided for FM and AM, independently.
- IF offset can be easily controlled at FM band.
- As serial ports are contained, control of all functions including frequency division number setting is performed through four serial bus lines.

MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC	SYMBOL	RATING	UNIT
Supply voltage	V_{DD}	-0.3 ∿6.0	V
Input voltage	V_{IN}	-0.3∿V_{DD}+0.3	V
Power Dissipation	P_D	300	mW
Operating Temperature	T_{opr}	-30 ∿75	°C
Storage Temperature	T_{stg}	-55 ∿125	°C

Unit in mm

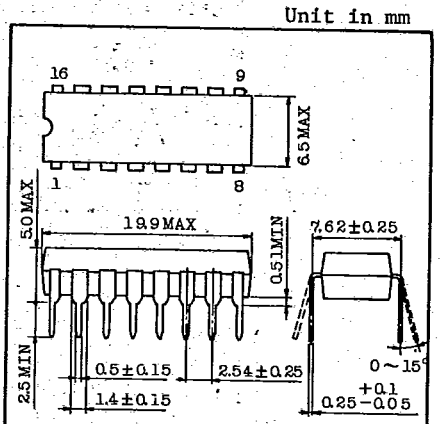


Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead trat is obtained on the basis of No.1 and No.22 leads.

JEDEC	—
TOSHIBA	4D22A-P

Weight: 2.06g

Unit in mm



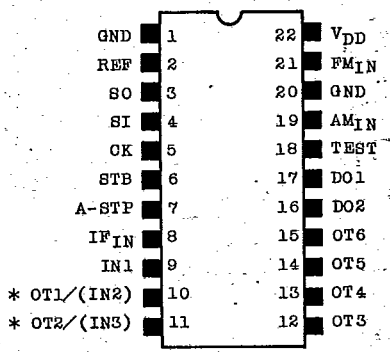
Lead pitch is 2.54 and tolerance is ±0.25 against theoretical center of each lead that is obtained on the basis of No.1 and No.16 leads.

JEDEC	—
TOSHIBA	3D16A-P

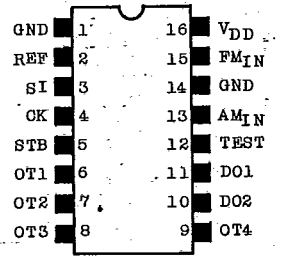
Weight : 1.0g

TC9171P, TC9172P, TC9182P-1

TERMINAL CONNECTION



TC9171P, TC9182P-1



TC9172P

Note: * Bracketed letters indicate TC9182P-1 terminal name.
Others indicate common terminals.

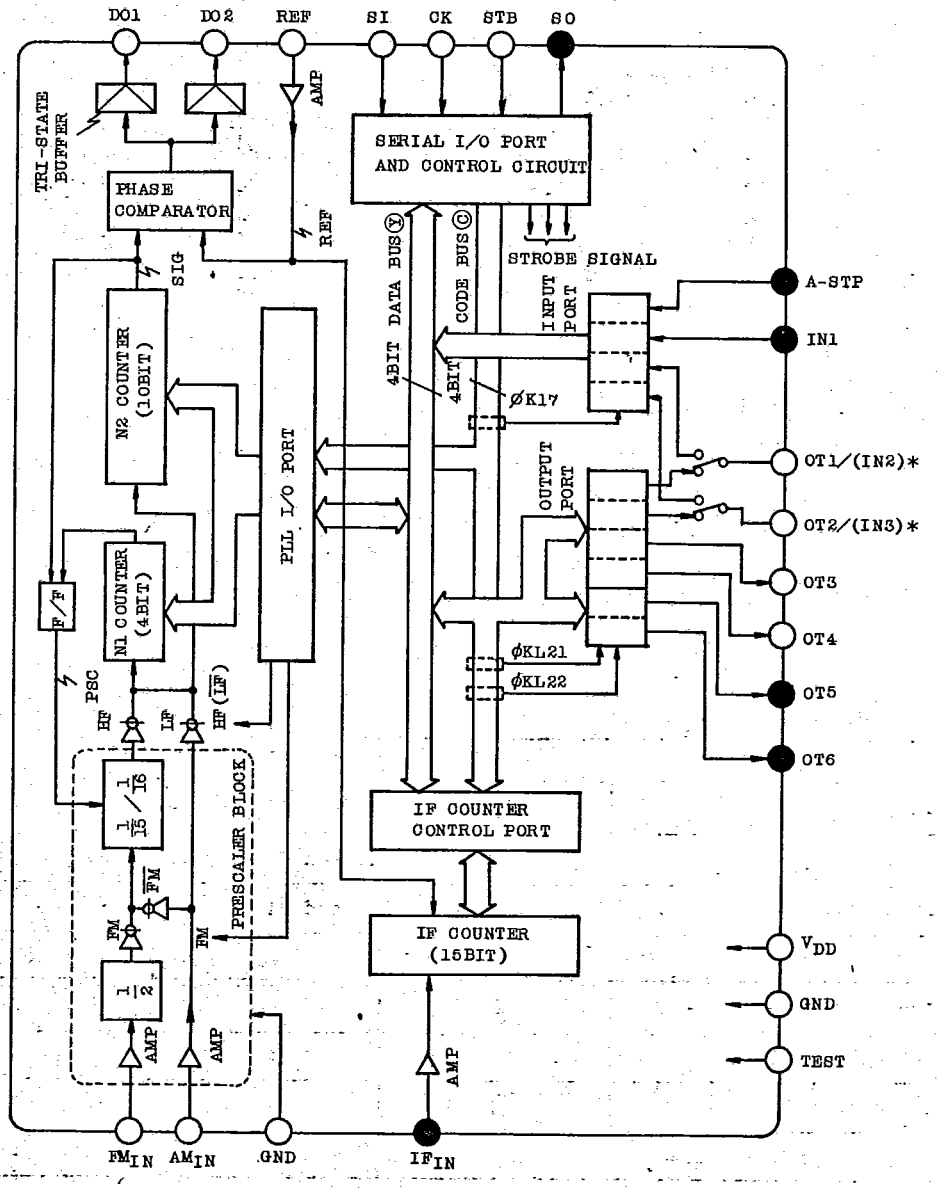
VERSION TABLE

Production name	TC9171P	TC9172P	TC9182P-1
Package	DIP 22 pin	DIP 16 pin	DIP 22 pin
Process	Silicon C^2MOS gate		
Frequency dividing type	Pulse swallow and direct dividing type		
Serial port	○	○	○
Input port	2	—	4
Output port	6	4	4
IF counter	○	—	○
Phase comparator output	2	2	2
Supply voltage	5V ± 10% single power supply		

TC9171P, TC9172P, TC9182P-1

BLOCK DIAGRAM

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Note: * Bracketed betters indicate TC9182P-1 terminal name. Others indicate TC9171P/82P-1 common terminals. ● Terminal does not exist in TC9172P.

TC9171P, TC9172P, TC9182P-1

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ELECTRICAL CHARACTERISTICS (Unless otherwise specified, Ta=25°C, V_{DD}=5V)

CHARACTERISTIC	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Operating Supply Voltage Range	V_{DD}	*	4.5	5.0	5.5	V
Operating Supply Current	I_{DD}	FM_{IN}=120MHz	-	15	25	mA
OPERATING FREQUENCY RANGE						
FM_{IN}	f_{FM}	V_{IN}=0.5Vpp *	50	~	140	MHz
AM_{IN} (HF mode)	f_{AMH}	V_{IN}=0.5Vpp *	8	~	30	MHz
AM_{IN} (LF mode)	f_{AML}	V_{IN}=0.3Vpp *	0.5	~	10	MHz
IF_{IN}	f_{IF}	V_{IN}=0.3Vpp *	0.4	~	13	MHz
REF Input	f_{REF}	V_{IN}=0.2Vpp *	1	~	100	kHz
OPERATING INPUT AMPLITUDE RANGE						
FM_{IN}	$V_{IN(FM)}$	f_{IN}=50~140MHz *	0.5	~	V_{DD}-0.5	Vpp
AM_{IN} (HF mode)	$V_{IN(AMH)}$	f_{IN}=10~30MHz *	0.5	~	V_{DD}-0.5	Vpp
AM_{IN} (LF mode)	$V_{IN(AML)}$	f_{IN}=0.5~10MHz *	0.3	~	V_{DD}-0.5	Vpp
IF_{IN}	$V_{IN(IF)}$	f_{IN}=0.4~13MHz *	0.3	~	V_{DD}-0.5	Vpp
REF Input	$V_{IN(REF)}$	f_{IN}=1~100kHz *	0.2	~	V_{DD}	Vpp
OT1~6, DO1~2, SO						
Output Current "H" Level	I_{OH}	V_{OH}=4V, SO terminal is excepted	-0.5	-1.0	-	mA
Output Current "L" Level	I_{OL}	V_{OL}=1V, SO terminal is excepted	0.5	1.0	-	mA
SO Terminal Output Current	I_{SO}	V_{OH}=4V	-2.0	-3.0	-	mA
SO Termianl Off Leak Current	I_{OFF}	V_{OUT}=0V	-	-	-1.0	μA
DO Terminal Tri-State Leakage Current	I_{TL}	V_{TLH}=5V, V_{TIL}=0V	-	-	±0.5	μA
IN1~3, SI, CK, STB, A-STP						
Input Current "H" Level	I_{IH}	V_{IH}=5V	-	-	1.0	μA
Input Current "L" Level	I_{IL}	V_{IL}=0V	-	-	-1.0	μA
Input Voltage "H" Level	V_{IH}		4.0	-	5.0	V
Input Voltage "L" Level	V_{IL}		0	-	1.0	V

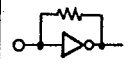
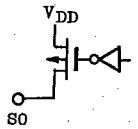
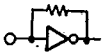
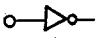
Note : * marked characteristics are guaranteed in a range of V_{DD}=4.5~5.5V, Ta=-30~75°C.

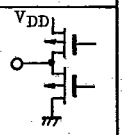
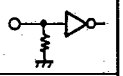
TC9171P, TC9172P, TC9182P-1

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FUNCTIONAL DESCRIPTION OF EACH TERMINAL

PIN No. ▭: Terminal of TC9172P, ▭: TC9171P/82P-1 Terminal

PIN No.	Symbol	Name terminal	Explanation of functions and operations	Remarks
2 2	REF	Reference frequency input	Input of reference frequency signal supplied from controller LSI. Built-in Amp. C coupling small amplitude operation.	
3 \	SO	Serial output	Serial I/O ports. Carries out between controller the setting of frequency dividing number, dividing type, and the transfer of data for controlling IF counter, general purpose I/O ports. As TC9172P has no serial output mode, SO terminal does not exist. SO terminal is Pch open drain output, and SI, CK, STB terminals are Schmitt trigger inputs.	  SI, CK, STB
4 3	SI	Serial input		
5 4	CK	Clock signal input		
6 5	STB	Strobe signal input		
7 \	A-STP	Auto stop input	Inputs auto stop signal. Can be used as general purpose input port also. (TC9171P/82P-1)	
8 \	IF_{IN}	IF signal input	IF signal input of IF counter to detect auto stop. Built-in Amp. C coupling small amplitude operation (TC9171P/82P-1).	
9 \	IN 1	General purpose input port	Freely usable general purpose input terminal (TC9171P/82P-1).	
10 6	OT1 *(IN2)	General purpose output ports	Freely usable general purpose output terminals. They can be used for switching control signal output of radio frequency circuit. · TC9171P : 6 · TC9172P : 4 · TC9182P-1 : 4 (Note)* In TC9182P-1, 10, 11 pins are indicated as input port.	
11 7	OT2 *(IN3)			
12 8	OT3			
13 9	OT4			
14 \	OT5			
15 \	OT6			

PIN No.	Symbol	Name terminal	Explanation of functions and operations	Remarks
16 10	DO2	Phase comparator outputs	Tri-state outputs of phase comparator. DO1, DO2 are parallel outputs.	
17 11	DO1			
18 12	TEST	Test terminal	Test mode control input. With pull-down resistance. Usually, used in OPEN state or GND connected.	
19 13	AM_{IN}	AM local oscillator signal input	Programmable counter input at AM band. Built-in Amp. C coupling small amplitude operation.	
20 14	GND	Prescaler block ground terminal	Grounding terminal for built-in prescaler.	
21 15	FM_{IN}	FM local oscillator signal input	Prescaler input at FM band. f_{Max} = 120 MHz Built-in Amp. C coupling small amplitude operation.	
22 16	V_{DD}	Power supply terminal	Supply 5V±10%.	
1 1	GND			

TC9171P, TC9172P, TC9182P-1

I/O MAP

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∘ TC9171P/82P-1

I/O / Code		PLL				General purpose output			
		Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8
INPUT PORT (K)	0	Programmable counter dividing type Setting							
		HF	ΔIF+1	ΔIF−1	FM				
	1	Programmable counter dividing number setting				General purpose output			
		P0	P1	P2	P3	OT1	OT2	OT3	OT4
	2	Programmable counter dividing number setting				General purpose output			
		P4	P5	P6	P7	OT5	OT6		
	3	Programmable counter dividing number setting							
		P8	P9	P10	P11				
	4	Programmable counter dividing number setting							
		P12	P13						
	5								
	6	IF counter control							
		BUSY	WIDE	STOP					
	7	General purpose output							
		A-STP	IN1	IN2	IN3				
OUTPUT PORT (L)	8	Programmable counter dividing type setting							
		HF	ΔIF+1	ΔIF−1	FM				
	9	Programmable counter dividing number setting				General purpose output			
		P0	P1	P2	P3	OT1	OT2	OT3	OT4
	A	Programmable counter dividing number setting				General purpose output			
		P4	P5	P6	P7	OT5	OT6		
	B	Programmable counter dividing number setting							
		P8	P9	P10	P11				
	C	Programmable counter dividing number setting							
		P12	P13						
	D	REF code data							
		1	3	4					
	E	IF counter control							
		START	WIDE	RESET					
	F	Chip select code data '1'				Chip select code data '2'			
		1	0	0	0	0	1	0	0

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∘ TC9172P

I/O / Code		PLL (1)				General purpose output (2)			
		Y1	Y2	Y4	Y8	Y1	Y2	Y4	Y8
INPUT PORT (K)	0								
	1								
	2								
	3								
	4								
	5								
	6								
	7								
OUTPUT PORT (L)	8	Programmable counter dividing type setting							
		HF	ΔIF+1	ΔIF−1	FM				
	9	Programmable counter dividing number setting				General purpose output			
		P0	P1	P2	P3	OT1	OT2	OT3	OT4
	A	Programmable counter dividing number setting							
		P4	P5	P6	P7				
	B	Programmable counter dividing number setting							
		P8	P9	P10	P11				
	C	Programmable counter dividing number setting							
		P12	P13						
	D								
	E								
	F	Chip select code data '1'				Chip select code data '2'			
		1	0	0	0	0	1	0	0

(Note) TC9172P contains no input port. As it contains no IF counter, there is no control port of it.

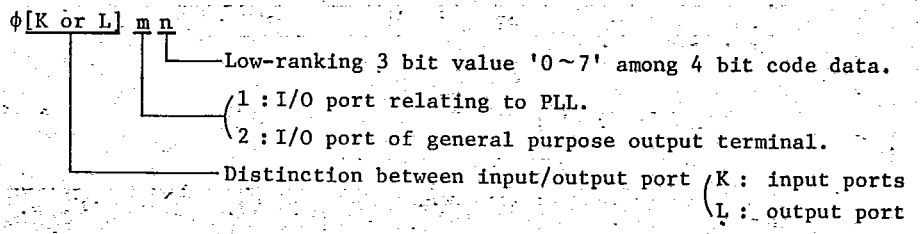
FUNCTIONAL DESCRIPTION

In TC9171P/72P/82P-1, as indicated in the block diagram, each function is controlled by accessing the ports connected with 4 bit data bus (Y) and code bus (C). Each data on this data bus and code bus is conducted from the controller LSI by four terminals of SI, SO, CK, STB (three terminals of SI, CK, STB in the case of TC9172P).

As control is all made with port, explanations will be given here chiefly about the functions of each port. These ports are constituted with 4-bit units, and are selected by 4-bit code data. Code assignment of each port is shown in I/O map indicated previously. On the whole, code '0H ∿ 7H' is assigned to input port, and code '8H ∿ FH' to output port.

(Note 1) "Input port" and "Output port" mentioned here are always based on the controller LSI. Thus, the port served when putting out data from controller LSI is called the output port, while the port (which data is taken from PLL side) to controller LSI is called the input port.

(Note 2) In this explanation, code assignment of each port is encoded as shown below.



(Example) ϕK17 : General purpose input port
ϕL21 : General purpose output ports OT1 ∿ OT4.

o Programmable counter

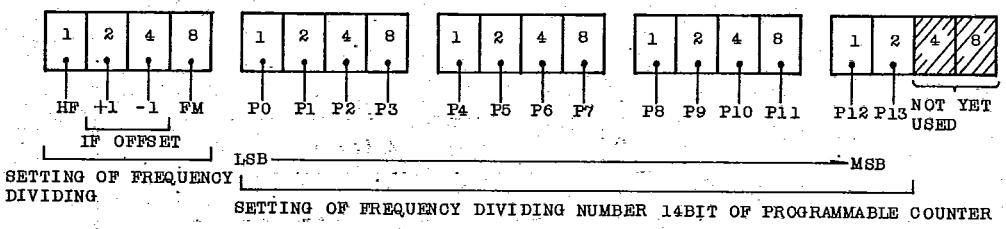
Programmable counter block is composed of two modulus prescaler, 4 bit + 10 bit programmable binary counter, and PLL I/O ports to control the above.

1. PLL I/O ports (ϕKL10 ∿ ϕKL14).

1) Exclusive PLL ports to entirely control frequency dividing number, dividing type and IF correction (IF offset) at FM band.

2) In TC9171P/82P-1, PLL ports are entirely of I/O port structure. Therefore, it is possible to take the set data again into the controller LSI by accessing input port. (ϕK10 ∿ ϕK14).

3) PLL port configuration.



4) Setting of frequency Dividing type.

Selection of pulse swallow dividing type or direct dividing type is made by HF, FM ports. Make selection from the following three types according to the applied frequency band.

HF	FM	Frequency Dividing type	Receiving band example	Input frequency range	Input terminal	Frequency Dividing number
0	0	Direct dividing	LW,MW,SW_L	0.5 ∿ 10 MHz	AM_{IN}	n
1	0	(1/15 /1/16) pulse swalllow type	SW_H	10 ∿ 30 MHz	AM_{IN}	n
0	1	Not use				
1	1	(1/2 ×1/15 /1/16) pulse swallow type	FM	50 ∿ 140 MHz	FM_{IN}	2·n

(Note) n represents programmed frequency dividing numeral value.

5) IF offset function at FM band

When pulse swallow dividing type is selected, it is possible to vary actual frequency dividing number by ± 1 without changing the programmed dividing numerals by ΔIFI1 ports. Thus, it can be applied to IF offset at FM band.

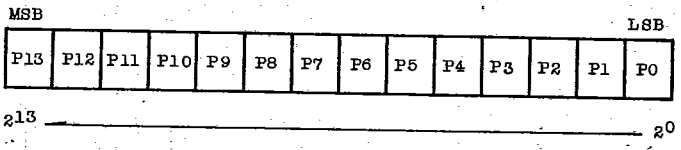
In the case of direct dividing type selection, IF off set function does not operate.

IF +1	IF -1	Frequency Dividing number (at FM bnad)
0	0	2·n
0	1	2·(n-1)
1	0	2·(n+1)
1	1	2·(n-1)

6) Setting of frequency Dividing number

Dividing number of programmable counter is set on $P_0 \sim P_{13}$ ports with binary.

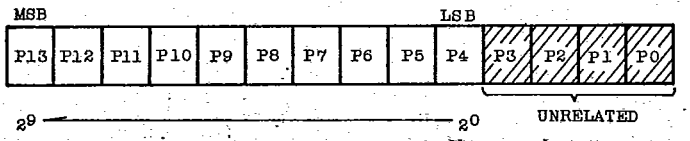
· At pulse swallow type (14 bit)



* Frequency dividing number setting range (pulse swallow type)

n = 210H ~ 3FFFH (528 ~ 16383)

· At direct dividing type (10 bit)



* Frequency dividing number setting range (Direct dividing type)

n = 10H ∿ 3FFH (16 ∿ 1023)

(Note 1) As the programmable counter is not provided with frequency dividing offset, the programmed dividing number becomes the actual frequency dividing number. However, in the case of FM band, the actual frequency dividing number becomes two times of programmed value.

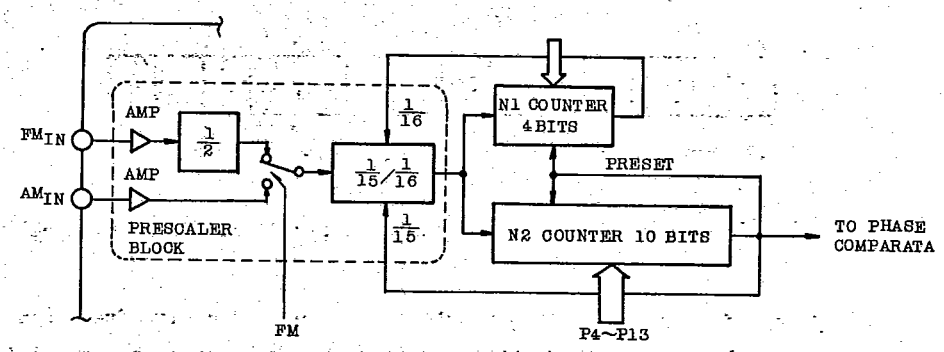
(Note 2) In the case of direct dividing type, P_0 ∿ P_3 port (ϕL11) datas become unrelated, and P_4 port becomes LSB.

(Note 3) Frequency dividing number is entirely renewed at the time of data setting of MSB port (ϕL14). For this reason, the data of MSB port (ϕL14) must be set at the end of dividing number setting. Even when the data setting is considered unnecessary (When the data is same as the previous one), the data setting must be executed for MSB port (ϕL14).

2. Circuit configuration of prescaler and programmable counter.

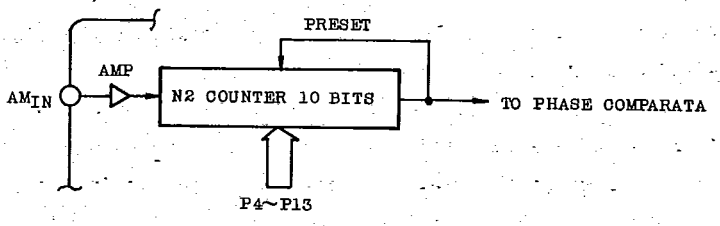
1) Circuit configuration of pulse swallow dividing type.

The circuit is composed of 1/15 /1/16 2-modulous prescaler and binary programmable counter of 4 bit on N1 side and 10 bit on N2 side.
In the case of FM band, 1/2 divider is added to the front stage of prescaler.



2) Circuit configuration of Direct dividing type

In this case, prescaler block is passed and N2 side counter 10 bits is used.



3) Both FM_{IN}, AM_{IN} terminals have built-in Amp, and small amplitude operation is possible with capacitor coupling.

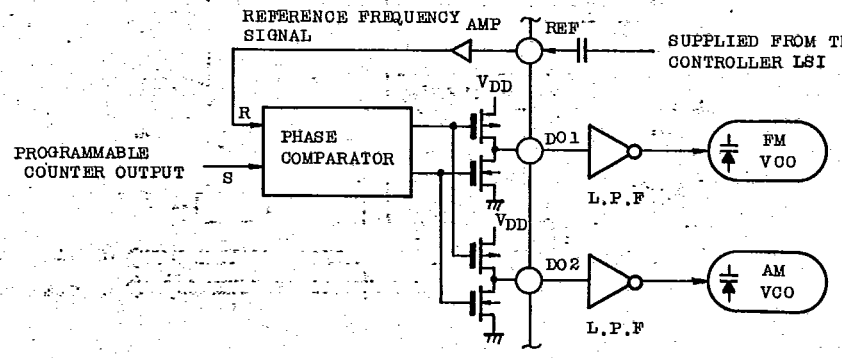
o Phase comparator

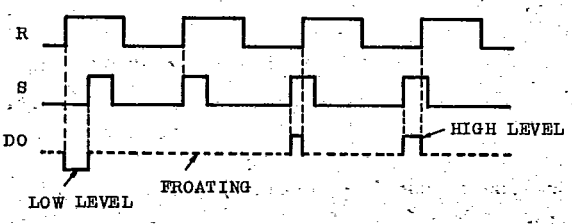
Phase comparator compares the phase difference between the reference frequency signal applied to REF terminal and programmable counter dividing output signal, and puts out its error component. Further, it controls VCO through low pass filter as that the frequency and phase of these two signals may agree with each other.

1) Two tri-state buffer DO1, DO2 terminals are put out in parallel from the phase comparator. For this reason, optimum design of filter constant can be made for each of FM/AM band.

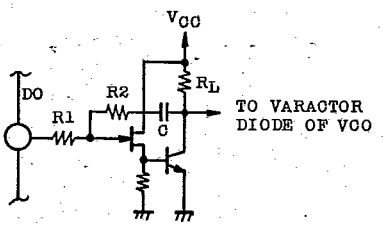
2) Reference frequency signal is supplied from the controller LSI to the REF terminal, and no crystal oscillator is needed on PLL LSI.

3) REF input has built-in amp, and small amplitude operation is possible with capacitor coupling.





DO output timing chart

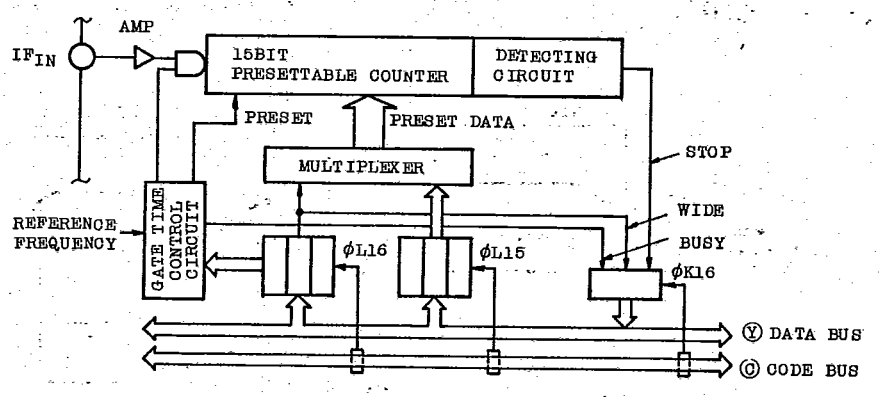


Example of active low pass filter

Above are indicated DO output timing chart and example of active low pass filter circuit by darlington connection of FET and transistor.

o IF Counter (TC9171P/82P-1)

TC9171P/82P-1 have IF counter which counts intermediate frequency (IF) of FM or AM during auto search tuning, and produces auto stop signal when that frequency has entered in the specified range. TC9172P contains no IF counter.
IF counter block is composed of 15 bit presettable counter and IF counter control ports.



1. Operation of IF counter

IF counter counts IF signal of 10.7 MHz at FM band and 450 kHz at AM band, and its gate-time is made of the reference frequency signal supplied to REF input.

1) IF_{IN} terminal has built-in Amp, and is capable of making small amplitude operation with capacitor coupling.

2) IF counter has two kinds of detectability, WIDE/NARROW.

3) Gate time and detectability in each band are shown below.

Band	Reference frequency (kHz)	NARROW		WIDE	
		Gate time (ms)	Detectability (Hz)	Gate time (ms)	Detectability (Hz)
LW	1	20	450K ± 600	5.0	450K ± 2.4K
SW	5	4.0	450K ± 3K	1.0	450K ± 12K
MW 9K	9	2.2	450K ± 5.4K	0.55	450K ± 21.6K
MW 10K	10	2.0	450K ± 6K	0.50	450K ± 24K
FM	12.5	1.6	10.7M ± 15K	0.4	10.7M ± 60K
	25	0.8		0.2	

·2. IF counter control output port

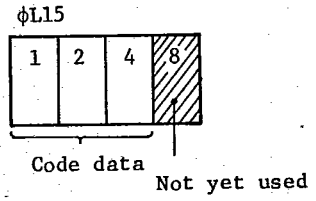
1) REF code data output port (φL15)

It sets the code data corresponding to the reference frequency which serves as time base. Never fail to set the code of the presently employed reference frequency signal.

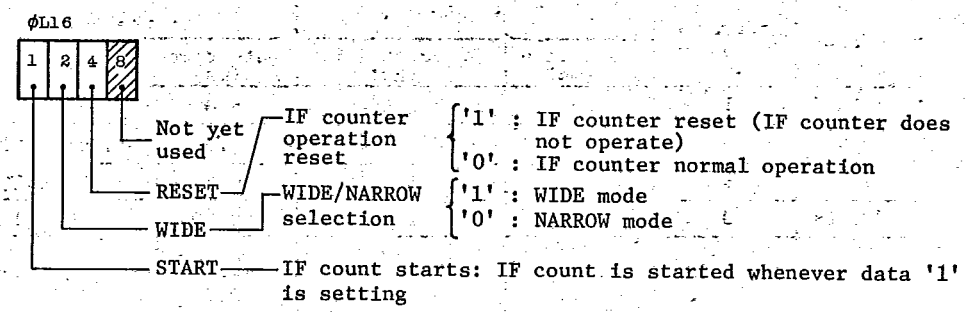
· Reference frequency code table

CODE DATA	0	1*	2	3*	4	5	6	7
Reference frequency	1K	50K	5K	100K	9K	10K	12.5K	25K

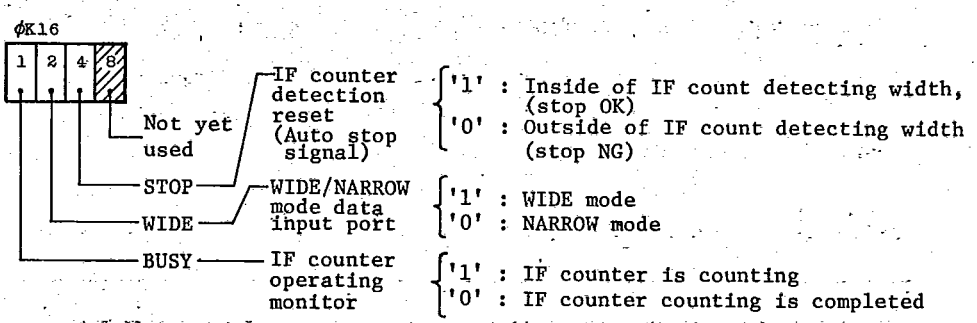
(Note) Code '1' and '3' can not use.



2) IF counter control output port (ϕL16)



3) IF counter control input port (ϕK16)



(Note 1) In the case of auto stop detection by IF counter, refer to the contents of STOP port after confirmation that BUSY port is '0' (counting completed).

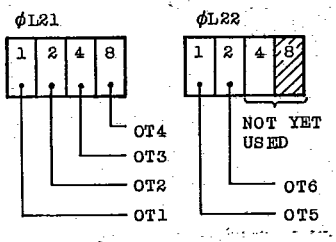
(Note 2) IF counter cannot be used when reference frequency of 50 kHz or 100 kHz is used at FM band or when IF off set is carried out. The same applies to the case where frequency other than 10.7 MHz and 450 kHz is used for IF signal.

o General purpose input and output ports

They have general purpose input/output terminals controlled with 4-bit units. However, TC9172P has output terminals only.

	Number of Input Terminal	Number of output Terminal
TC9171P	2	6
TC9172P	—	4
TC9182P-1	4	4

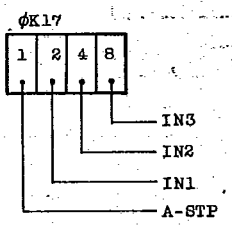
1) General purpose output ports (ϕL21, ϕL22)



(Note) TC9172P has no ϕL22 port.
In the case of TC9182P-1, OT1, OT2 ports are not put out to terminals.

The set data is put out in positive logic.
Output terminals are CMOS structure. In TC9171P/82P-1, general purpose output ports are entirely of I/O ports structure. Therefore, it is possible to take the set data again into the controller side by accessing input ports (ϕK21, ϕK22).

2) General purpose input port (ϕK17)



(Note 1) In TC9171P, data of IN2, IN3 ports is '0'. Further, TC9172P has no general purpose input port.

(Note 2) A-STP port is for auto stop signal input use, but it can be applied to other use.

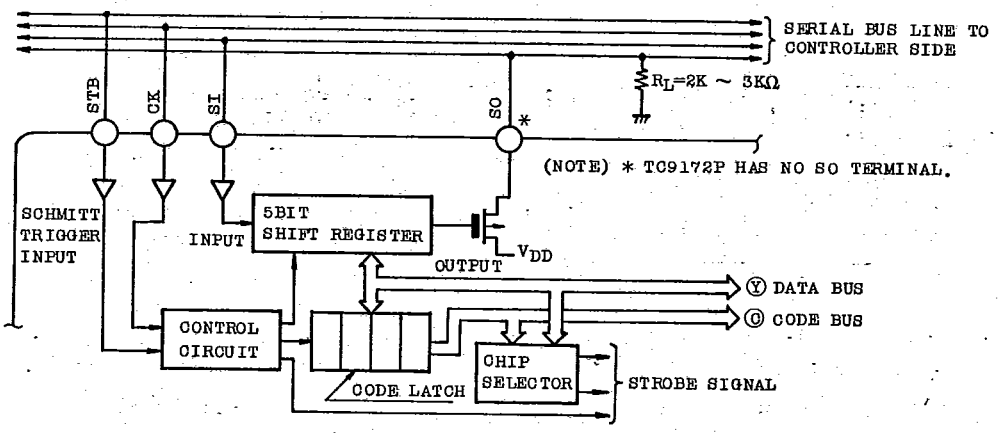
Data is got in positive logic. Input terminals are CMOS structure.

o Serial I/O ports

As shown previously, each port is controlled through serial ports and serial bus line. Serial ports control the data transfer between the serial bus line and code data bus line of IC inside.

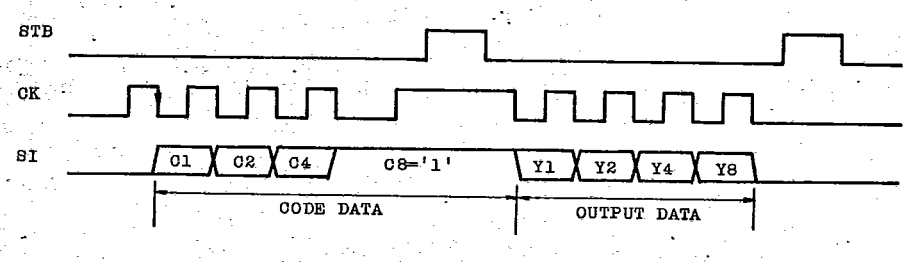
Number of input/output terminals of serial port is as follows:
TC9171P/82P-1 ... 4 terminals (SO, SI, CK, STB), with input port.
TC9172P ..... 3 terminals (SI, CK, STB), without input port.
SI, CK, STB terminals contain Schmitt trigger input, and SO terminal has P-ch FET open drain output construction.

(Note) SO terminal needs external load resistance. (R_L=2k ~ 3kΩ)



1. Data transfer format

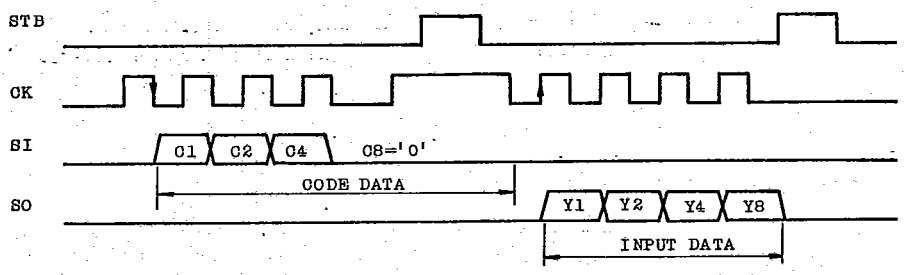
1) Data output timing (access of output port)



Code data (C1 ∿ C8) 4 bits of output port and output data (Y1 ∿ Y8) 4 bits are serially transferred to SI terminal with the timing shown above. SI data is read in with the rising of CK.

(Note) During the designation of output port, code data 'C8' is '1' at all times.

2) Data input timing (access of input port)



When code data (C1 ∿ C8) 4 bits of input port is transferred to SI terminal with the above timing, the data of designated port is output to SO terminal with 4 bit serial of Y1 ∿ Y8. SI data is read in with the rising of CK signal, and SO data is putout with the rising of CK signal.

(Note) During the designation of input port, code data 'C8' is '0' at all times.

2. Designation of chip select

Besides PLL IC, various peripheral option ICs can be connected on the serial bus line. It is sucessary, therefore, to designate the IC connected with controller LSI through bus line, between which data is to be transferred. Chip select code is provided to designate the controlled IC on the bus line.

Select code for designating TC9171P/72P/82P-1 is as follows:

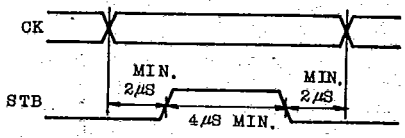
* Chip select code for PLL I/O ports : 1
* Chip select code for general purpose output ports : 2

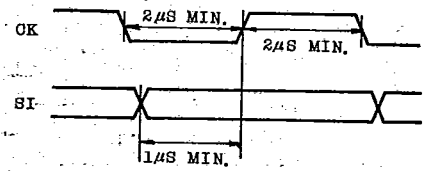
1) Select code is set up to the chip select code data output port. (code 'FH')

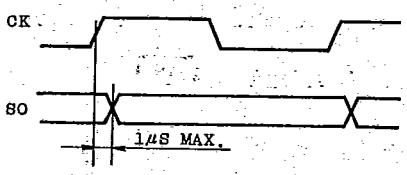
2) Select code must be set up first at the time of serial data transfer.

3) Select code once set maintains the same data unless otherwise designated, and so, there is no need of designating select code every time serial data is transferred.

3. Pulse width of serial timing



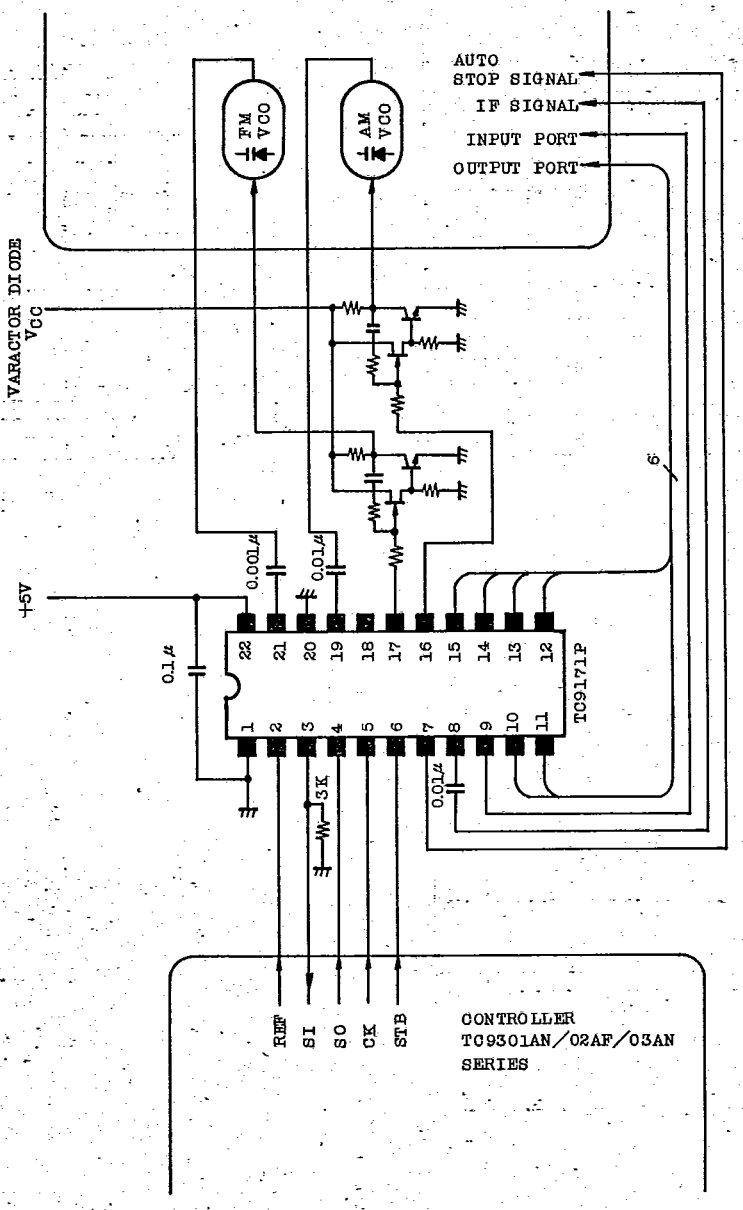




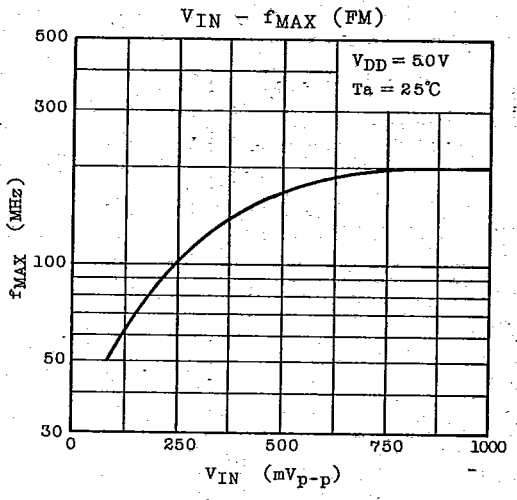
TC9171P, TC9172P, TC9182P-1

EXAMPLE FOR APPLICATION CIRCUIT

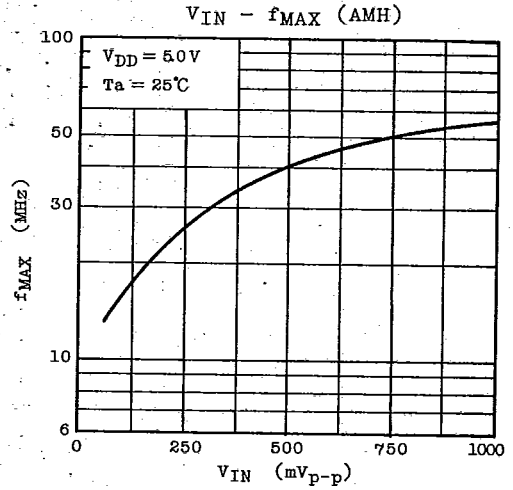
T-50-17



V_{IN} – f_{MAX} (FM)



V_{IN} – f_{MAX} (AMH)



V_{IN} – f_{MAX} (AML)

