TA8115N/F

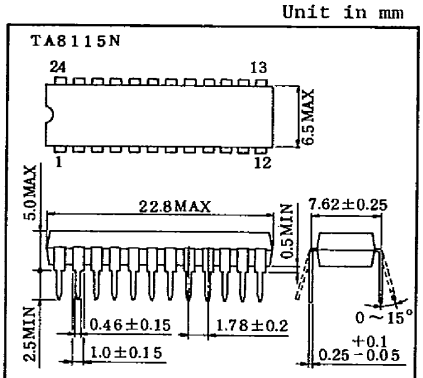
TENTATIVE

DUAL PRE-AMPLIFIERS + HEADPHONE DRIVERS
FOR AUTOREVERSE SYSTEM IC (3V USE)

The TA8115N/F are developed for auto reverse play back headphone cassette play (3V use).
The pre-amplifiers are independent of the headphone drivers, the voltage gains of which are fixed at 27dB(Typ.).

- Switchover between Forward/Reverse input mode is possible with only one-make switch.
- Built-in Metal/Normal equalizer drivers, switchover between Metal/Normal equalizer mode is possible with only one-make switch. Those drivers are applicable to LED driver for Forward/Reverse directional display, too.
- Operating supply voltage range.
  $V_{CC(opr)}$=1.8~6V (Ta=25°C)

Unit in mm

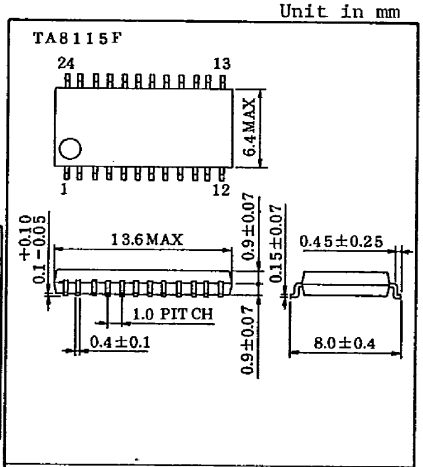


Lead pitch is 1.78 and tolerance is ±0.2 against theoretical center of each lead that is obtained on the basis of No.1 and No.24 leads.

JEDEC	—
TOSHIBA	3D24C-P

Weight : 1.2g

Unit in mm



JEDEC	—
TOSHIBA	F24GD-P

Weight : 0.31g

MAXIMUM RATINGS (Ta=25°C)

CHARACTERISTIC		SYMBOL	RATING	UNIT
Supply Voltage		V_{CC}	6	V
Power Dissipation (Note)	TA8115N	P_D	1200	mW
	TA8115F		400	
Operating Temperature		Topr	-25~75	°C
Storage Temperature		Tstg	-55~150	°C

Note: Derated above Ta=25°C in the proportion of 9.6mW/°C for TA8115N, and of 3.2mW/°C for TA8115F.

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ELECTRICAL CHARACTERISTICS

(Unless otherwise specified. V_{CC}=3V, f=1kHz, R_L=16Ω, Ta=25°C)

CHARACTERISTIC		SYMBOL	TEST CIR-CUIT	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Quiescent Current		I_{CCQ}	1	V_{IN}=0	-	9	16	mA
Pre-Amplifier Section	Open Loop Voltage Gain	G_{VO}	1	V_{OUT}=-10dBm	68	80	-	dB
	Maximum Output Voltage	V_{OM}	1	THD=1%	300	450	-	mVrms
	Total Harmonic Distortion	THD1	1	V_{OUT}=-10dBm	-	0.02	0.1	%
	Equivalent Input Noise Voltage	V_{NI}	1	Rg=2.2kΩ BW=20Hz~20kHz NAB(G_V=33dB, f=1kHz)	-	0.9	1.5	μVrms
	Ripple Rejection Ratio	RR1	1	Vrip=-10dBm f=100Hz, Rg=2.2kΩ	45	60	-	dB
	Input Bias Current	IB1	3	V_{IN}=0	-	0.5	1.5	μA
	Cross Talk (Forward/Reverse)	CT_{FR}	1	V_{OUT}=-10dBm Rg=2.2kΩ BW=20Hz~20kHz	63	73	-	dB
Headphone Driver Section	Output Power	P_{OUT}	1	THD=10%, R_L=16Ω	38	50	-	mW
	Closed Loop Voltage Gain	GVC	1	V_{OUT}=-10dBm	25	27	29	dB
	Total Harmonic Distortion	THD2	1	P_{OUT}=1mW	-	0.3	2.0	%
	Output Noise Voltage	V_{NO}	1	Rg=600Ω BW=20Hz~20kHz	-	25	70	mVrms
	Ripple Rejection Ratio	RR2	1	Vrip=-10dBm f=100Hz, Rg=600Ω	45	60	-	dB
	Input Resistance	R_{IN}	1	-	-	20	-	kΩ
	Input Bias Current	IB2	3	V_{IN}=0, Rg=100kΩ	-	5	40	nA
	Channel Balanse	CB	1	V_{OUT}=-10dBm	-	-	1	dB
	ON-Resistance of Metal Driver	R_{ON}	2	-	-	20	-	Ω
	Maximum LED Current	I_{LED}	4	V_{CE}=0.3V	3.5	-	-	mA
Pre + Driver	Cross Talk (L/R)	CT_{LR}	1	V_{OUT}=-5dBm(Driver) BW=20Hz~20kHz	40	53	-	dB
	Signal Leakage	SL	1	V_{OUT}=12dBm(Pre) BW=20Hz~20kHz	55	63	-	dB

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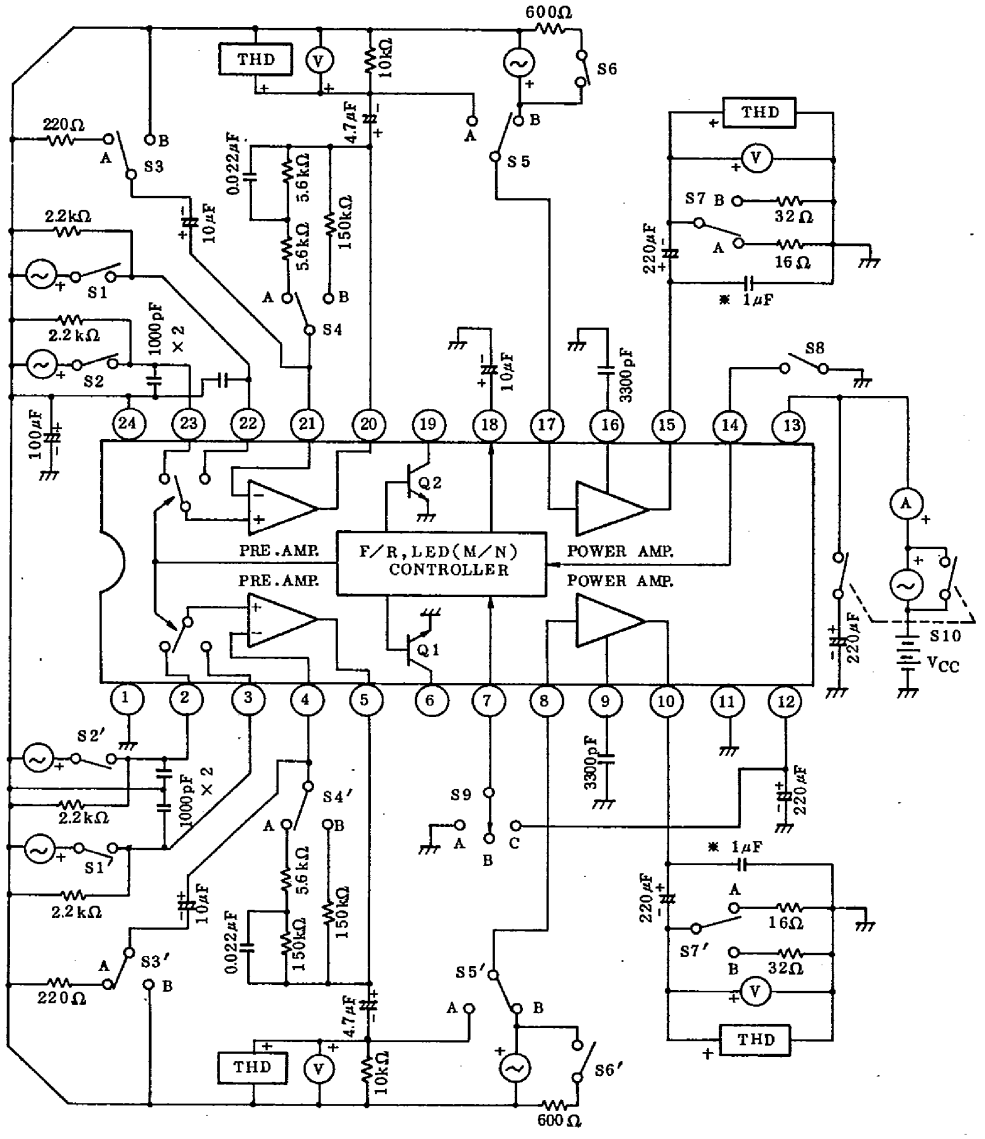
TEST CIRCUIT]



* : Monolithic ceramic condenser

* See the "switch state for electrical characteristics".

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SWITCH STAGE FOR ELECTRICAL CHARACTERISTICS

× ..... OFF, ○ ..... ON

SW / Characteristic	S1	S1′	S2	S2′	S3	S3′	S4	S4′	S5	S5′	S6	S6′	S7	S7′	S8	S9	S11
I_{CCQ}	×	×	×	×	A	A	A	A	B	B	○	○	A	A	×	B	○
G_{VO}	○	○	○	○	B	B	B	B	B	B	○	○	A	A	○/×	B	○
THD 1	○	○	○	○	A	A	A	A	B	B	○	○	A	A	○/×	B	○
V_{OM}	○	○	○	○	A	A	A	A	B	B	○	○	A	A	○/×	B	○
V_{NI}	×	×	×	×	A	A	A	A	B	B	○	○	A	A	○/×	B	○
CT_{FR}	○/×	○/×	×/○	×/○	A	A	A	A	B	B	○	○	A	A	×↔○	B	○
P_{OUT}	×	×	×	×	A	A	A	A	B	B	×	×	A	A	×	B	○
G_{VC}	×	×	×	×	A	A	A	A	B	B	×	×	A	A	×	B	○
THD 2	×	×	×	×	A	A	A	A	B	B	×	×	A	A	×	B	○
V_{NO}	×	×	×	×	A	A	A	A	B	B	○	○	A	A	×	B	○
CB	×	×	×	×	A	A	A	A	B	B	×	×	A	A	×	B	○
CT_{LR}	○/×	×/○	○/×	×/○	A	A	A	A	A	A	×	×	A	A	×	B	○
SL	○	○	○	○	A	A	A	A	A	A	×	×	A	A	×	B	○
RR 1	×	×	×	×	A	A	A	A	B	B	○	○	A	A	×	B	×
RR 2	×	×	×	×	A	A	A	A	B	B	○	○	A	A	×	B	×

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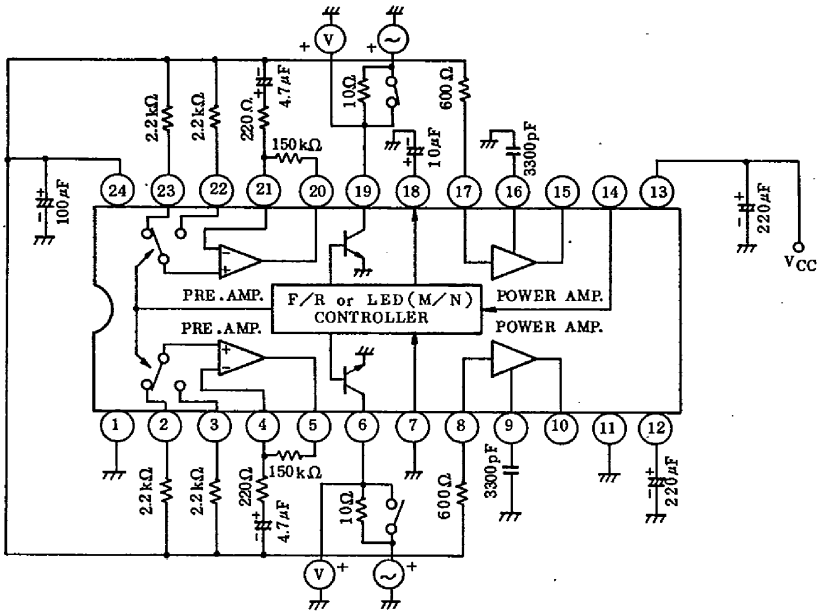
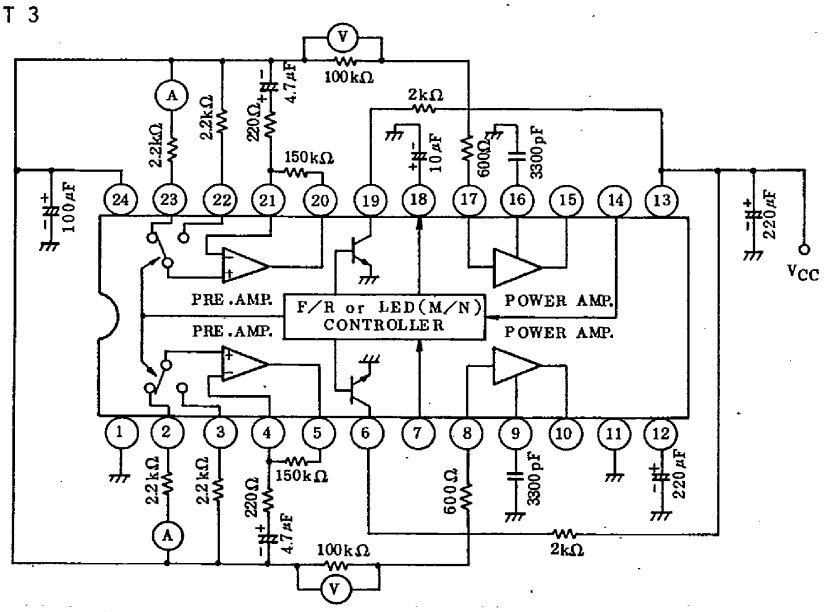
TEST CIRCUIT 2



TEST CIRCUIT 3



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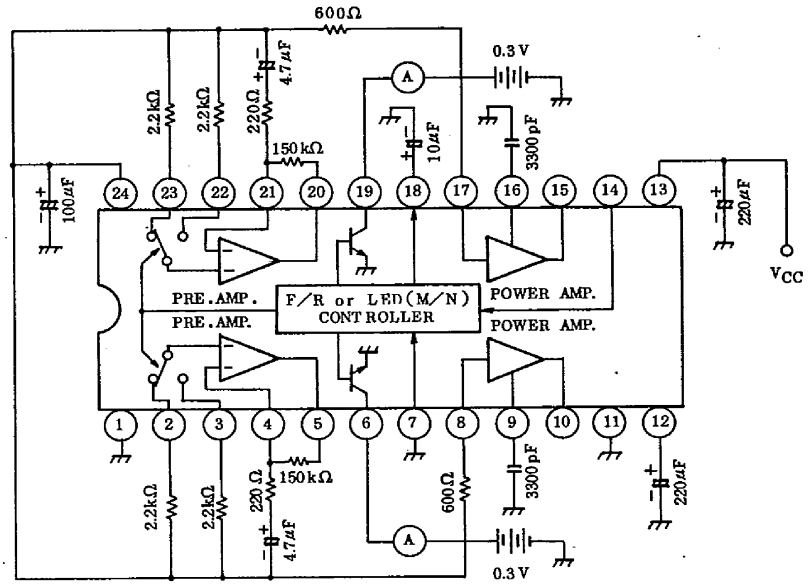
TEST CIRCUIT 4



FUNCTION MODE TABLE (See "TEST CIRCUIT-1")

This IC is set to the mode shown in the table below, by the state of the control terminals, pin 7, pin 14.

S9	S8	Q1	Q2	PRE AMPLIFIER INPUT TERMINAL	APPLICABLE FUNCTION
C	OFF	OFF	ON	Pin 2, Pin 23	Tape Directional Display
C	ON	ON	OFF	Pin 3, Pin 22	
B	OFF	OFF	OFF	Pin 2, Pin 23	EQ ; Normal
B	ON	OFF	OFF	Pin 3, Pin 22	
A	OFF	ON	ON	Pin 2, Pin 23	EQ : Metal
A	ON	ON	ON	Pin 3, Pin 22	

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DC CHARACTERISTICS

(V_{CC}=3V, V_{IN}=0, R_L=16Ω, Ta=25°C, TEST CIRCUIT-5) (Unit : V)

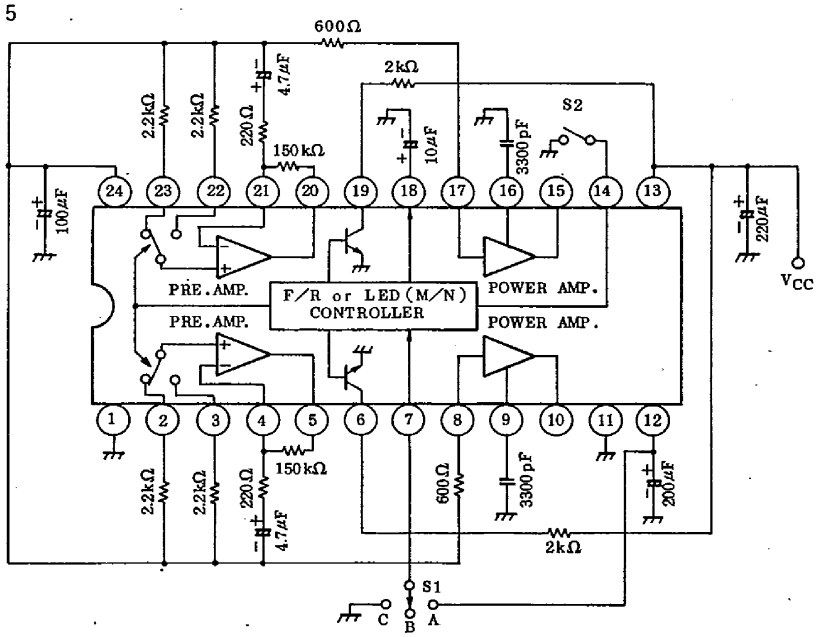
TERMINAL No.	1	2	3	4	5	6	7	8	9	10	11	12
Terminal Voltage	0	1.5	1.5	1.5	1.5	Note	Note	1.5	0.7	1.5	0	2.6

TERMINAL No.	13	14	15	16	17	18	19	20	21	22	23	24
Terminal Voltage	3.0	Note	1.5	0.7	1.5	Note	Note	1.5	1.5	1.5	1.5	1.5

Note: These terminals are set to the voltages shown in the table below, by the control switches S1, S2.

SWITCH MODE		TERMINAL VOLTAGE (V)				
S1	S2	Pin 6	Pin 7	Pin 14	Pin 18	Pin 19
A	OFF	3.0	2.6	0.6	0	<0.3
	ON	<0.3	2.6	0	0.6	3.0
B	OFF	3.0	0.2	0.6	0	3.0
	ON	3.0	0.2	0	0.6	3.0
C	OFF	<0.3	0	0.6	0	<0.3
	ON	<0.3	0	0	0.6	<0.3

TEST CIRCUIT 5



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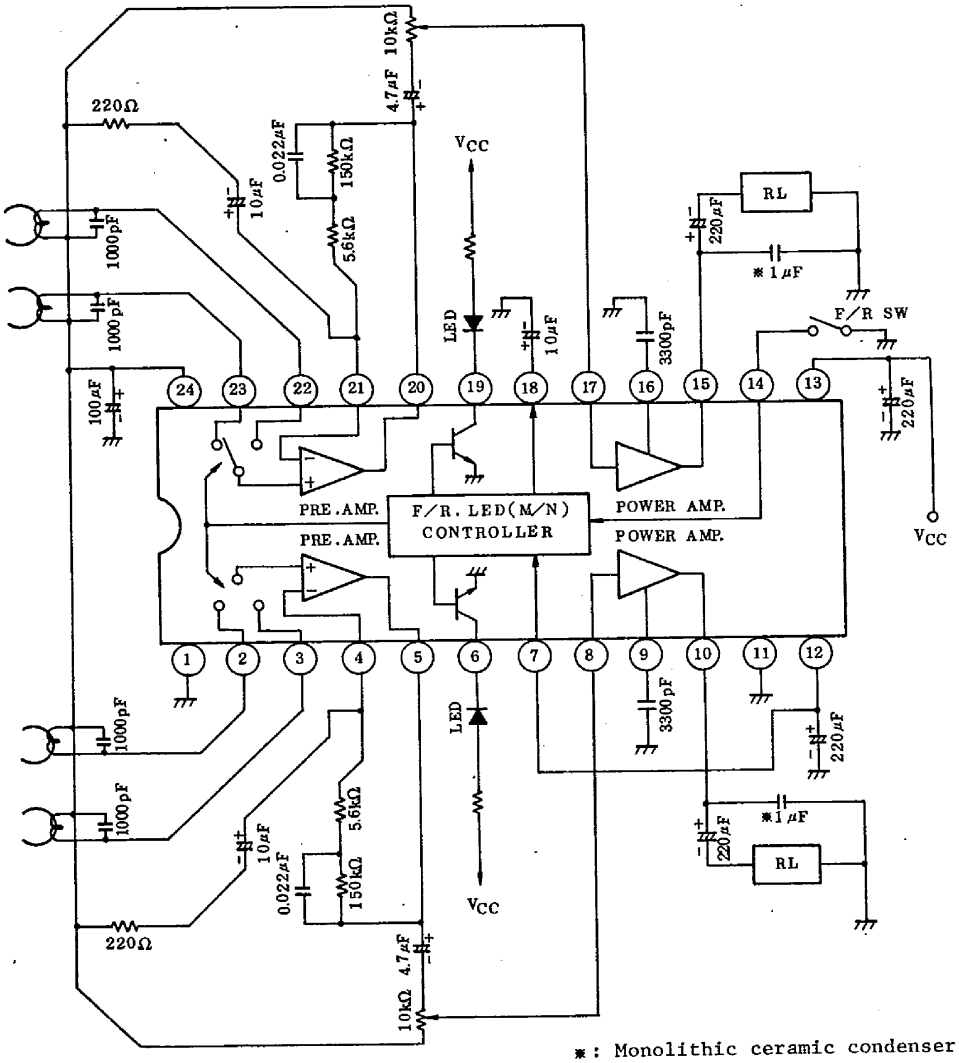
APPLICATION CIRCUIT 1 (Tape directional display for LED)



*: Monolithic ceramic condenser

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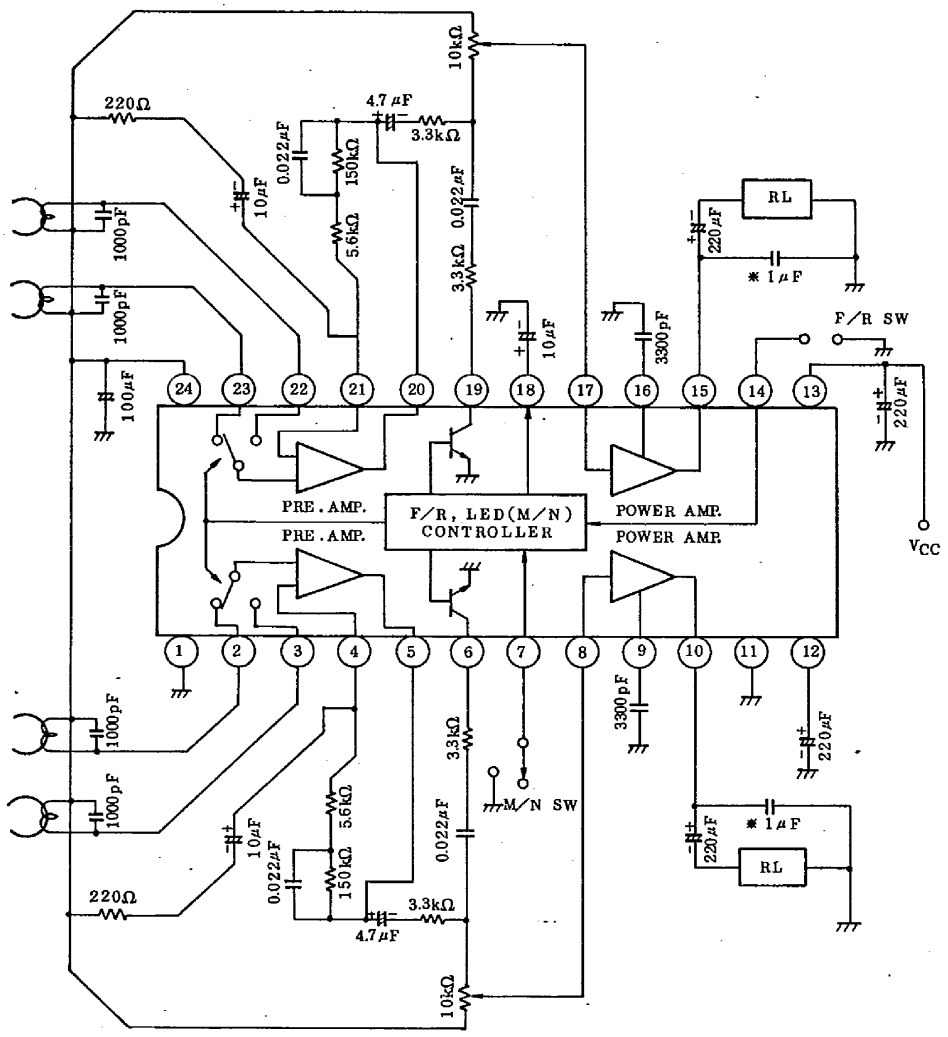
APPLICATION CIRCUIT 2 (Equalizer switchover between Normal/Metal mode)



* : Monolithic ceramic condenser

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APPLICATION NOTE FOR PATTERN LAYOUT

(1) The GND line of pin 1 (Pre GND) must be isolated from that of pin 11 (PW GND) at the GND point, where the V_{CC} decoupling condenser C9 is placed.

(2) The GND line of C1 (for Ripple Filter) must be isolated from that of condenser C2 (for Reference Voltage), at the point of pin 1.

(3) The pattern diagram between the pin 24 (terminal of V_{REF}) and the condenser C2 must be made shortly. As for the pin 1 (Pre GND), it's as well.

(4) The pattern diagram between the pin 11 (PW GND) and the compensation condenser, C6 must be shortly. And this positive line of C6 must be kept away from the terminals of PW IN, pin 8, 17.

(5) The lines of PW IN must be kept away from those of PW OUT. And each of the PW OUT lines must be kept away.

(6) The line of PW GND (pin 11) must be isolated from the load GND lines, at the GND point, where the V_{CC} decoupling condenser C9.

(7) The GND lines of condensers C8, which are for compensation of radiation, must be isolated from other GND lines to pin 11.

* See the example of pattern layout as shown next page.

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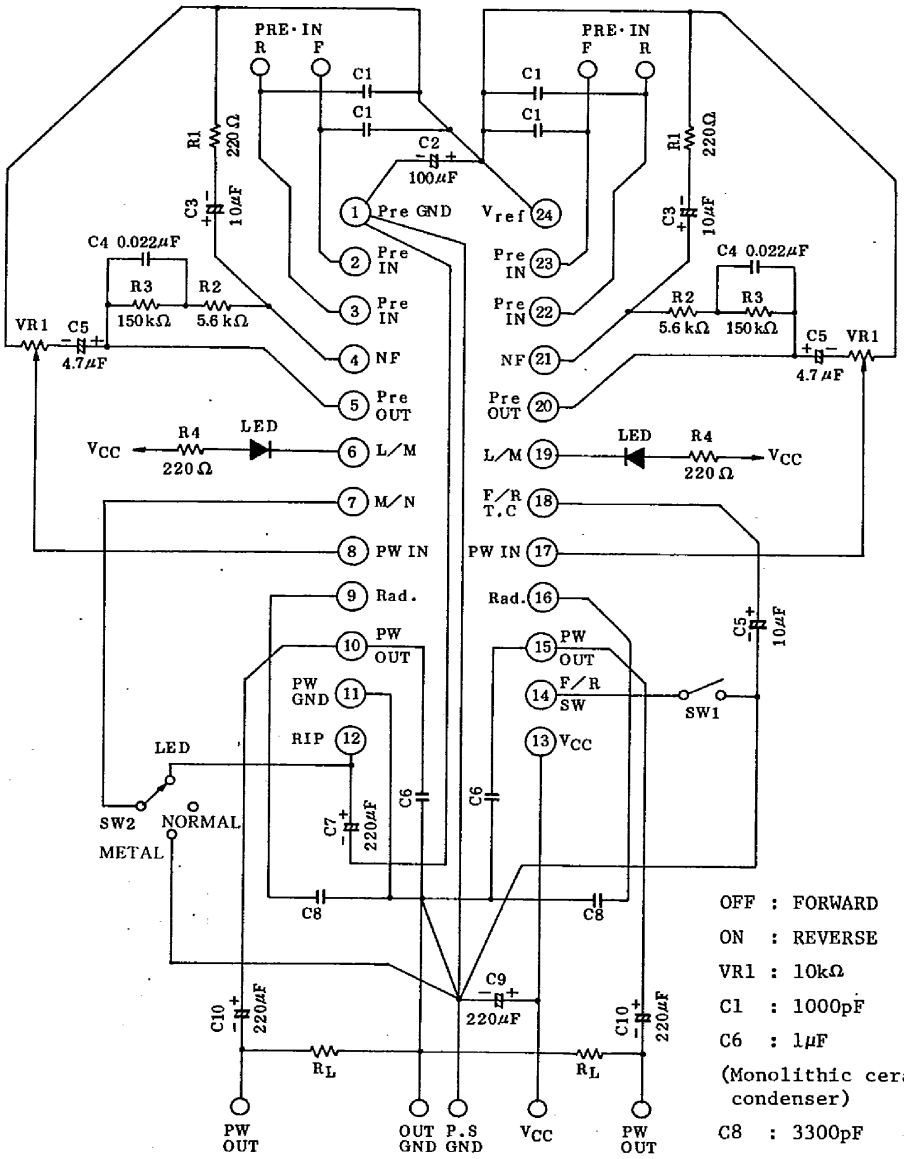
AN INSTANCE FOR RECOMMENDED PCB PATTERN LAYOUT



OFF : FORWARD
ON : REVERSE
VR1 : 10kΩ
C1 : 1000pF
C6 : 1μF
(Monolithic ceramic condenser)
C8 : 3300pF

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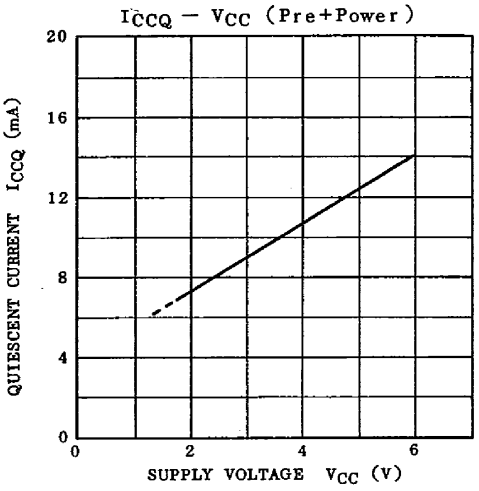
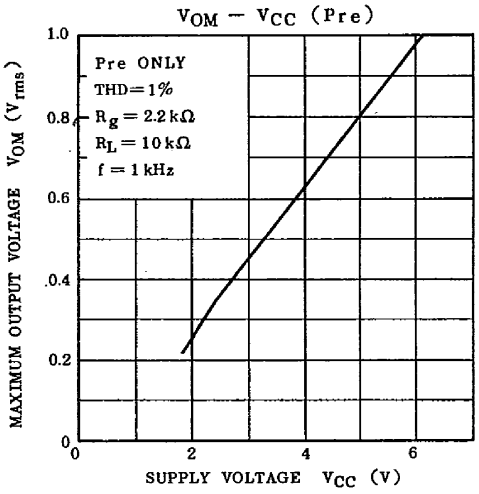
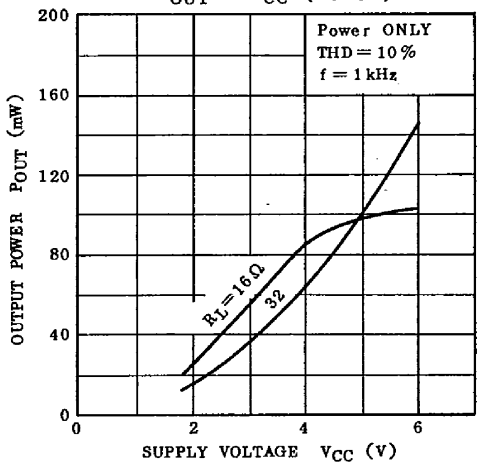
I_{CCQ} – V_{CC} (Pre+Power)



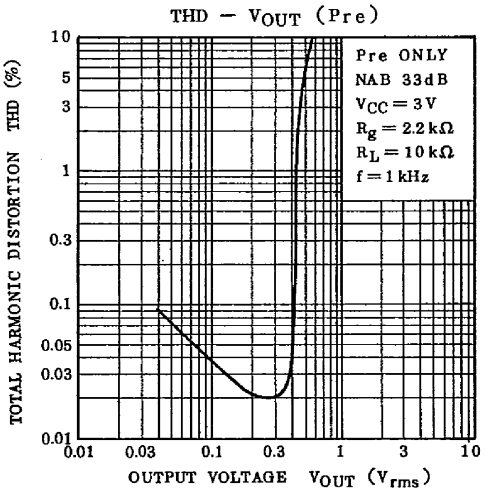
V_{OM} – V_{CC} (Pre)



P_{OUT} – V_{CC} (Power)



THD – V_{OUT} (Pre)



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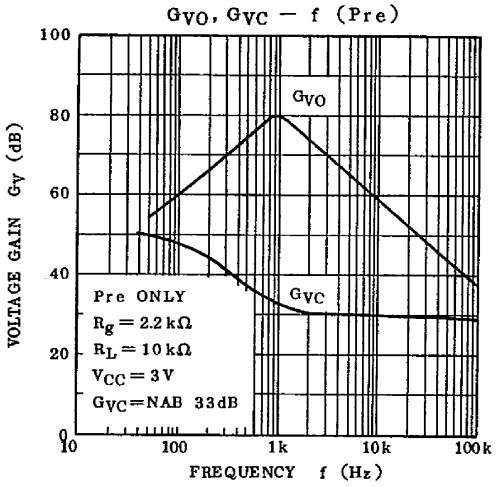
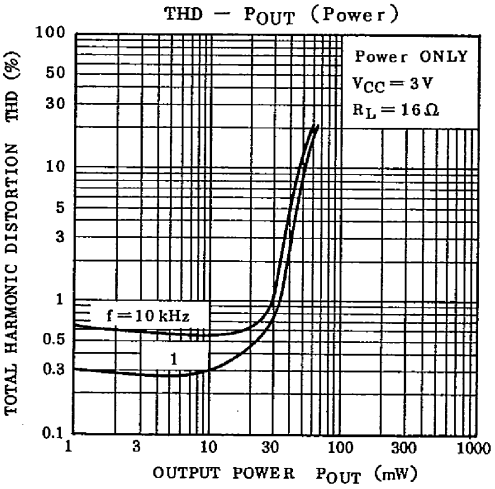
G_{VO}, G_{VC} — f (Pre)



THD — P_{OUT} (Power)



G_{VO} — f (Power)