SYSTEM CONTROLLER AND BUS DRIVER FOR M5L 8080A P, S CPU

DESCRIPTION

The M5L 8228P is a system controller and bus driver for M5L 8080A P, S CPUs. It generates all signals required to directly interface the MELPS 8 series RAMs, ROMs and input/output devices. A bidirectional bus driver, along with system control signals, provides for high system TTL fan-out. It is fabricated using Schottky TTL technology.

FEATURES

- Built-in bidirectional bus driver for data bus isolation
- Built-in status signal
- High system TTL fan-out
- User selected single level interrupt vector (RST 7)
- Interchangeable with Intel's 8228 in terms of pin configuration and electrical characteristics

APPLICATION

- Data bus driver and status signal generation for M5L 8080A P, S CPU

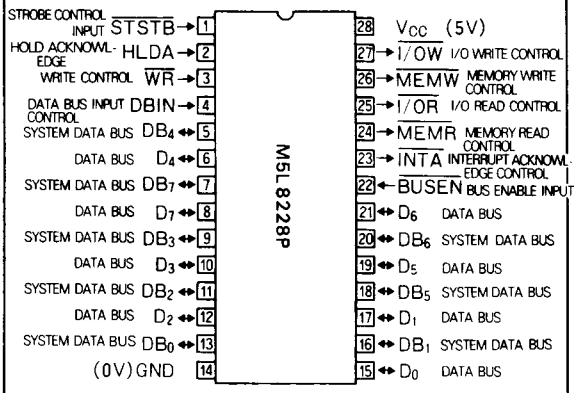
FUNCTION

The bidirectional bus driver provides high system TTL fanout, as well as isolation for an M5L 8080A P, S CPU data bus from memory and I/O devices.

Status signals from a CPU are latched in the internal status latch when the status strobe signal $\overline{STSTB}$ goes low. The gating array generates control signals (memory read $\overline{MEMR}$, memory write $\overline{MEMW}$, input/output read $\overline{I/OR}$, input/output write $\overline{I/OW}$, and interrupt acknowledge $\overline{INTA}$) by gating the output of the status latch with the control signals DBIN, $\overline{WR}$ and HLDA from a CPU. The bus enable input $\overline{BUSEN}$ forces the data bus output buffers and control signal buffers to high-impedance state if they are in the high-state.

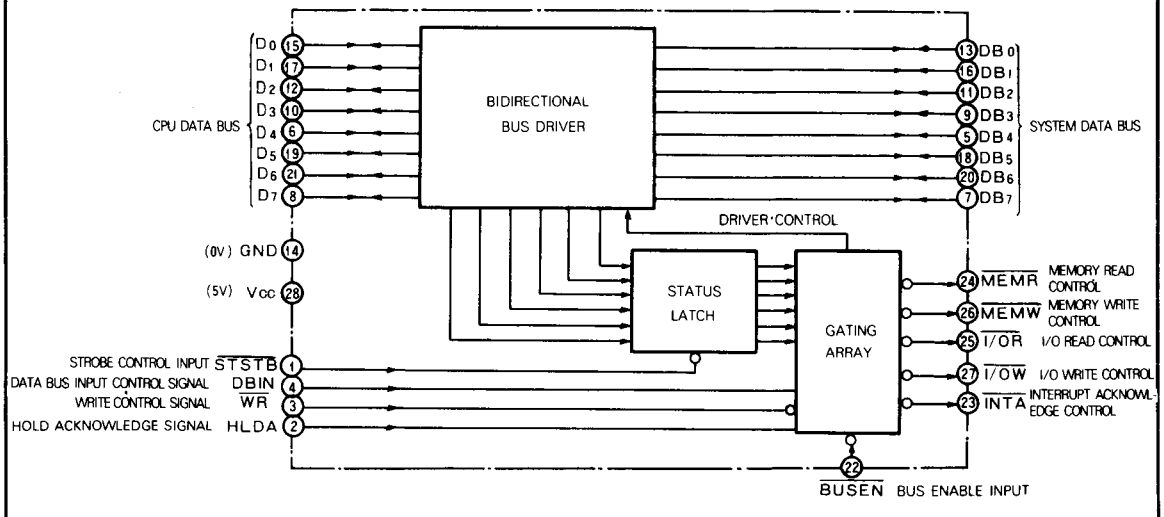
An RST 7 instruction gated to the bus as an interrupt is acknowledged when the DBIN input is active and a 12V supply in series with a 1kΩ resistor is connected to the acknowledge output $\overline{INTA}$.

PIN CONFIGURATION (TOP VIEW)



Outline 28P1

BLOCK DIAGRAM



SYSTEM CONTROLLER AND BUS DRIVER FOR M5L 8080A P, S CPU

SUMMARY OF OPERATIONS

Bidirectional Bus Driver

An 8-bit bidirectional bus driver is provided to buffer the data bus of the M5L8080A CPU from the memory and I/O devices. Its flow is controlled by the gating array. The system data bus output is provided with ample load-driving capacity ($I_{OL}=10mA$). It can be turned to the high-impedance state by the bus enable ($\overline{BUSEN}$) input in order to separate the memory and I/O devices from the CPU.

Status Latch

Latches status information from the CPU and is used in deriving the memory and I/O control signals. Status information from CPU terminals $D_0 \sim D_7$ is latched at the rising edge of $\overline{STSTB}$. Terminal $\overline{STSTB}$ is usually connected to output terminal $\overline{STSTB}$ of the M5L8224P clock generator.

FUNCTION OF THE STATUS SIGNALS

Data bus	Signal name	Status information	Functions
D_0	INTA	Interrupt acknowledge	Turns high when CPU acknowledges interrupt request by INT.
D_1	$\overline{WO}$	Write mode discriminating	Turns high when CPU is in read mode, and turns low when in write mode.
D_2	STACK	Stack	Turns high during that part of the machine cycle when the value in the stack pointer, that is, the address of the push down stack is output on the address bus.
D_3	HLTA	HLT instruction acknowledge	Turns high during that part of the machine cycle when the CPU halts on executing the HLT instruction.
D_4	OUT	Output instruction acknowledge	Turns high during that part of the machine cycle when the output port number is carried to the address bus and the data is carried to the data bus. The output port number is output on both the upper and lower eight bits of the address bus at the same time.
D_5	M_1	M_1	Turns high during that part of the machine cycle when the CPU fetches the first byte to the instruction.
D_6	INP	Input instruction acknowledge	Turns high during that part of the machine cycle when the input port number is carried to the address bus and the data bus becomes the input mode. The input port number is output on both the upper and lower eight bits of the address bus at the same time.
D_7	MEMR	Memory read	Turns high during that part of the machine cycle when the data bus is utilized to fetch the memory contents.

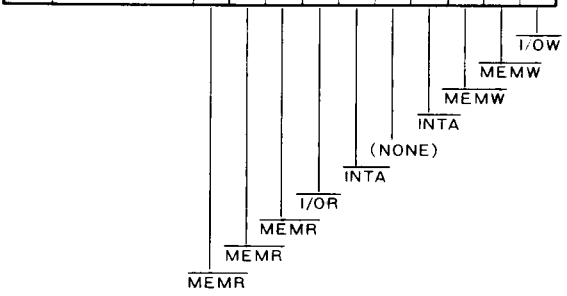
Gating Array

Memory and I/O control signals are generated from this circuit after logically combining the contents of the status latch and signals DBIN, $\overline{WR}$ and HLDA from the CPU.

The relationship between the CPU status information and the M5L8228P control signal is tabulated below.

STATUS INFROMATION AND THE TYPES OF THE MACHINE CYCLES

Status information \ Mode number	1	2	3	4	5	6	7	8	9	10
Data bus bit / Name of status signal	Instruction fetch	Memory read	Stack read	Input read	Interrupt acknowledge	HALT acknowledge	Interrupt acknowledge while HALT	Memory write	Stack write	Output write
D_0 INTA	0	0	0	0	1	0	1	0	0	0
D_1 $\overline{WO}$	1	1	1	1	1	1	1	0	0	0
D_2 STACK	0	0	1	0	0	0	0	0	1	0
D_3 HLTA	0	0	0	0	0	1	1	0	0	0
D_4 OUT	0	0	0	0	0	0	0	0	0	1
D_5 M_1	1	0	0	0	1	0	1	0	0	0
D_6 INP	0	0	0	1	0	0	0	0	0	0
D_7 MEMR	1	1	1	0	0	1	0	0	0	0



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Use Of Terminal $\overline{INTA}$

1. When Interrupt Instruction is Applied Externally

Fig. 1 Typical external interrupt instruction

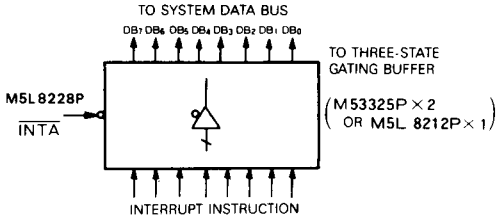
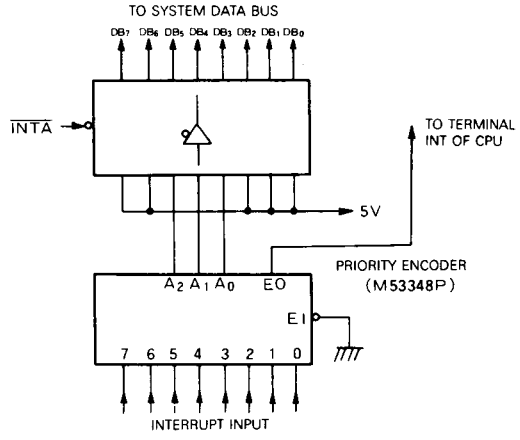


Fig. 2 In case priority is given to an interrupt instruction



2. When Interrupt Instruction is Generated from the M5L 8228P

When terminal $\overline{INTA}$ is connected to the 12V line through a 1kΩ resistance, an instruction coded "FF_{16}" (RST 7) is automatically generated on the CPU data bus at the next DBIN which follows the cycle when the CPU issued the $\overline{INTA}$ status (interrupt acknowledge).

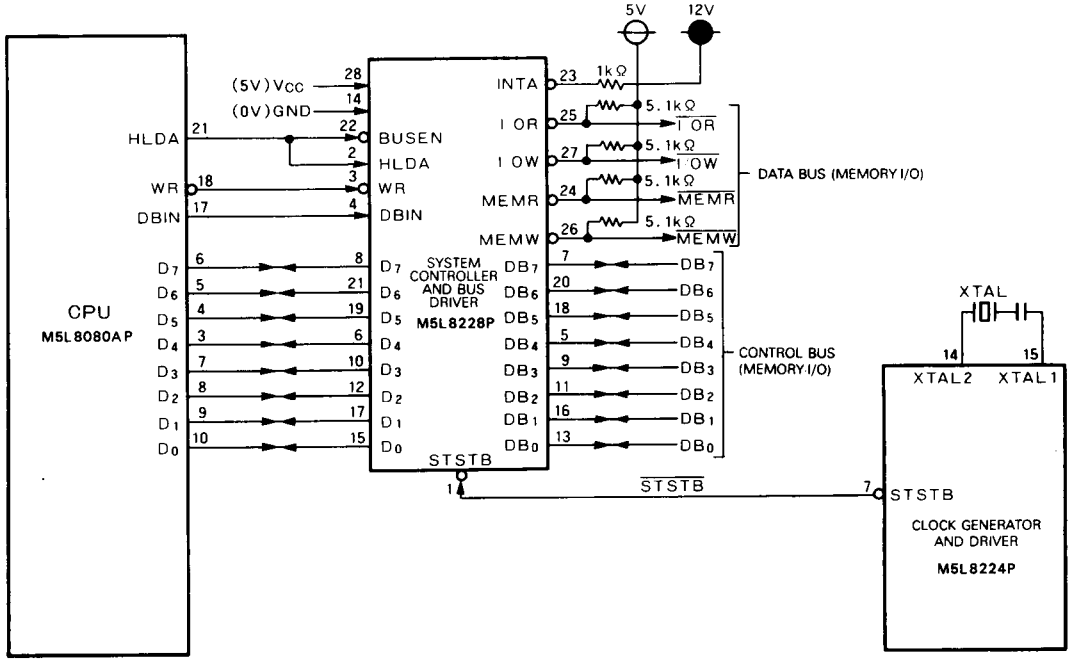
State After Initial Power-On Time

State of the status latch within the M5L 8228P is unstable immediately after the initial power-on, however, the $\overline{STSTB}$ signal is sent to the M5L 8228P when the M5L 8224P clock generator sends the reset signal to the CPU. Even if the CPU data bus is in the high-impedance state at this time, $D_2 = D_6 =$ "1" is latched, as the pull-up resistance is connected with D_2 and D_6 in the M5L 8228P. As the internal flip-flop is reset this way, there will not be any unrequired control signals being issued during the power-on time.

Use of Terminal $\overline{BUSEN}$

Fig.3 shows typical M5L 8228P connection. When terminal $\overline{BUSEN}$ turns high-level, all the data bus buffers and control output buffers of the M5L 8228P turn to the high-impedance state. Therefore, the data and control buses of the system can be controlled externally when signal HLDA (hold acknowledge) is issued from the CPU as the HOLD request was applied to the CPU, if the terminal HLDA of the CPU is connected with the terminal $\overline{BUSEN}$ of the M5L 8228P. This feature is very useful in direct memory accessing DMA.

Fig. 3 Typical M5L 8228P connection



SYSTEM CONTROLLER AND BUS DRIVER FOR M5L 8080A P, S CPU

ABSOLUTE MAXIMUM RATINGS (Ta = 0 ~ 75°C, unless otherwise noted)

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage		7.0	V
V_I	Input voltage, $D_0 \sim D_7$ and $\overline{STSTB}$ input		V_{CC}	V
V_I	Input voltage, all other inputs		7.0	V
V_O	Output voltage		V_{CC}	V
P_d	Power dissipation		1.0	W
Topr	Operating free-air temperature		0 ~ 75	°C
Tstg	Storage temperature		−55 ~ 125	°C

RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 75°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5.0	5.25	V
I_{OH}	High-level output current, $D_0 \sim D_7$ outputs			−10	μA
I_{OH}	High-level output current, all other outputs			−1	mA
I_{OL}	Low-level output current, $D_0 \sim D_7$ outputs			2	mA
I_{OL}	Low-level output current, all other outputs			10	mA

ELECTRICAL CHARACTERISTICS (Ta = 0 ~ 75°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.0			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Input clamp voltage	V_{CC} = 4.75V, I_{IC} = −5mA			−1.0	V
V_{OH}	High-level output voltage, $D_0 \sim D_7$ outputs	V_{CC} = 4.75V, V_{IH} = 2.0V, V_{IL} = 0.8V, I_{OH} = −10μA	3.6			V
	High-level output voltage, all other outputs	V_{CC} = 4.75V, V_{IH} = 2.0V, V_{IL} = 0.8V, I_{OH} = −1mA	2.4			
V_{OL}	Low-level output voltage, $D_0 \sim D_7$ outputs	V_{CC} = 4.75V, V_{IH} = 2.0V, V_{IL} = 0.8V, I_{OL} = 2mA			0.5	V
	Low-level output voltage, all other outputs	V_{CC} = 4.75V, V_{IH} = 2.0V, V_{IL} = 0.8V, I_{OL} = 10mA			0.5	
I_{OZ}	Three-state output current	V_{CC} = 5.25V, V_{IH} = 2.0V, V_{IL} = 0.8V, V_O = 5.25V			20	μA
	Three-state output current	V_{CC} = 5.25V, V_{IH} = 2.0V, V_{IL} = 0.8V, V_O = 0.5V			−20	
I_{IH}	High-level input current, $\overline{STSTB}$ input	V_{CC} = 5.25V, V_{IH} = 4.5V, V_{IL} = 0V, V_I = 5.25V			100	μA
	High-level input current, $DB_0 \sim DB_7$ inputs				20	
	High-level input current, all other inputs				100	
I_{IL}	Low-level input current, $\overline{STSTB}$ input	V_{CC} = 5.25V, V_{IH} = 4.5V, V_{IL} = 0V, V_I = 0.5V			−0.5	mA
	Low-level input current, D_2, D_6 inputs				−0.75	
	Low-level input current, D_0, D_1, D_4, D_5, D_7 inputs				−0.25	
	Low-level input current, all other inputs				−0.25	
I_{OS}	Short-circuit output current (Note 3)	V_{CC} = 5.0V, V_{IH} = 4.5V, V_{IL} = 0V	−15		−90	mA
$I_{I(\overline{INTA})}$	$\overline{INTA}$ terminal current	V_{DD} = 12V, R_L = 1kΩ ± 10%			5	mA
I_{CC}	Supply current from V_{CC}	V_{CC} = 5.25V, V_{IH} = 4.5V, V_{IL} = 0V			190	mA

Note 1 : All voltages are with respect to GND terminal. Reference voltage (pin 14) is considered as 0V, and all maximum and minimum values are defined in absolute values.

2 : Current flowing into an IC is positive; out is negative. The maximum and minimum values are defined in absolute values.

3 : All measurements should be done quickly, and two outputs should not be measured at the same time.

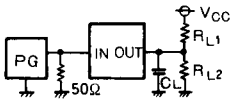
TIMING REQUIREMENTS (Ta = 0 ~ 75°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{w(\overline{STSTB})}$	$\overline{STSTB}$ pulse width		22			ns
$t_{su(DA)}$	$D_0 \sim D_7$ setup time with respect to $\overline{STSTB}$		8			ns
$t_{su(DB)}$	$DB_0 \sim DB_7$ setup time with respect to HLDA		10			ns
$t_{h(DA)}$	$D_0 \sim D_7$ hold time with respect to $\overline{STSTB}$		5			ns
$t_{h(DB)}$	$DB_0 \sim DB_7$ hold time with respect to HLDA		20			ns

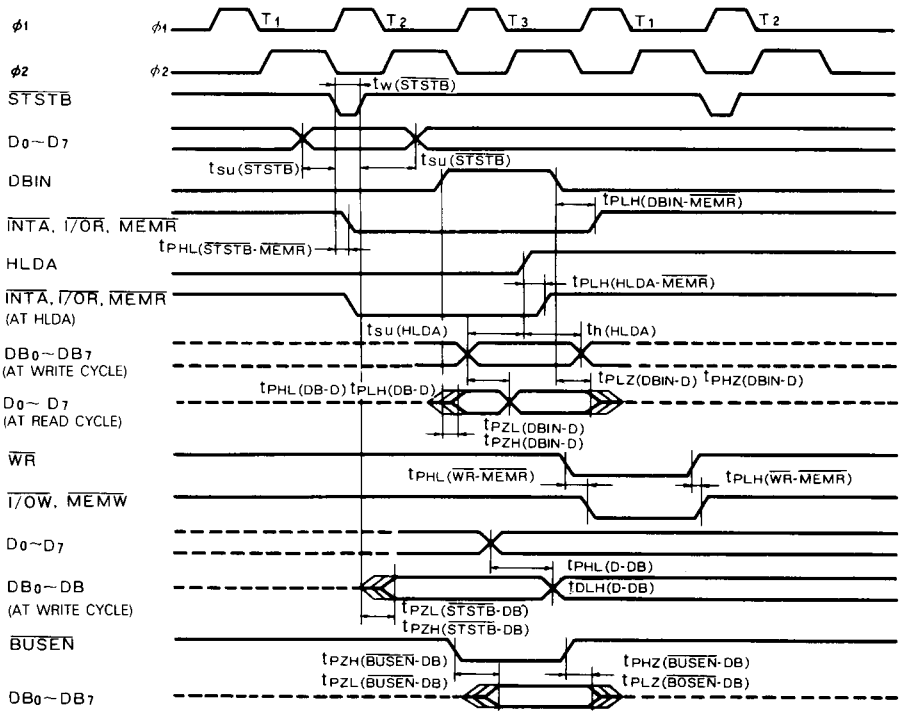
SWITCHING CHARACTERISTICS ($T_a = 25°C$, $V_{CC} = 5V$, unless otherwise noted)

	Parameter	Test conditions (Note 4)	Limits			
			Min	Typ	Max	
$t_{PHL(\overline{STSTB}\text{-}\overline{MEMR})}$	High-to-low-level output propagation time, from input $\overline{STSTB}$ to output $\overline{MEMR}$, $\overline{I/OR}$ and $\overline{INTA}$	$V_{IH} = 4.5V$, $V_{IL} = 0V$, $C_L = 100pF$, $R_{L1} = 500\Omega$, $R_{L2} = 1k\Omega$	20		70	ns
$t_{PLH(DBIN\text{-}\overline{MEMR})}$	Low-to-high-level output propagation time, from input DBIN to output $\overline{MEMR}$, $\overline{I/OR}$ and				40	ns
$t_{PZL(DBIN\text{-}D)}$ $t_{PZH(DBIN\text{-}D)}$ $t_{PHZ(DBIN\text{-}D)}$ $t_{PLZ(DBIN\text{-}D)}$	Z-to-low-level, Z-to-high-level, high-to-Z-level and low-to-Z-level output propagation time, from input DBIN to outputs $D_0 \sim D_7$	$C_L = 25pF$, $R_{L1} = 4k\Omega$, $R_{L2} = \infty\Omega$			55	ns
$t_{PHL(DB\text{-}D)}$ $t_{PLH(DB\text{-}D)}$	High-to-low-level and low-to-high-level output propagation time, from inputs $DB_0 \sim DB_7$ to outputs $D_0 \sim D_7$				40	ns
$t_{PHL(\overline{WR}\text{-}\overline{MEMW})}$ $t_{PLH(\overline{WR}\text{-}\overline{MEMW})}$	High-to-low-level and low-to-high-level output propagation time, from input $\overline{WR}$ to outputs $\overline{MEMW}$ and $\overline{I/OW}$	$C_L = 100pF$, $R_{L1} = 500\Omega$, $R_{L2} = 1k\Omega$	5		55	ns
$t_{PZL(\overline{STSTB}\text{-}DB)}$ $t_{PZH(\overline{STSTB}\text{-}DB)}$	Z-to-low-level and Z-to-high-level output propagation time, from input $\overline{STSTB}$ to outputs $DB_0 \sim DB_7$				40	ns
$t_{PHL(D\text{-}DB)}$ $t_{PLH(D\text{-}DB)}$	High-to-low-level and low-to-high-level output propagation time, from inputs $D_0 \sim D_7$ to outputs $DB_0 \sim DB_7$		5		50	ns
$t_{PZL(\overline{BUSEN}\text{-}DB)}$ $t_{PZH(\overline{BUSEN}\text{-}DB)}$ $t_{PHZ(\overline{BUSEN}\text{-}DB)}$ $t_{PLZ(\overline{BUSEN}\text{-}DB)}$	Z-to-low-level, Z-to-high-level, high-to-Z-level and low-to-Z-level output propagation time, from input $\overline{BUSEN}$ to outputs $DB_0 \sim DB_7$				40	ns
$t_{PLH(HLDA\text{-}\overline{MEMR})}$	Low-to-high-level output propagation time, from input HLDA to outputs $\overline{MEMR}$, $\overline{I/OR}$ and $\overline{INTA}$				35	ns

Note 4 Measurement circuit:



TIMING DIAGRAM REFERENCE LEVEL = 1.5V



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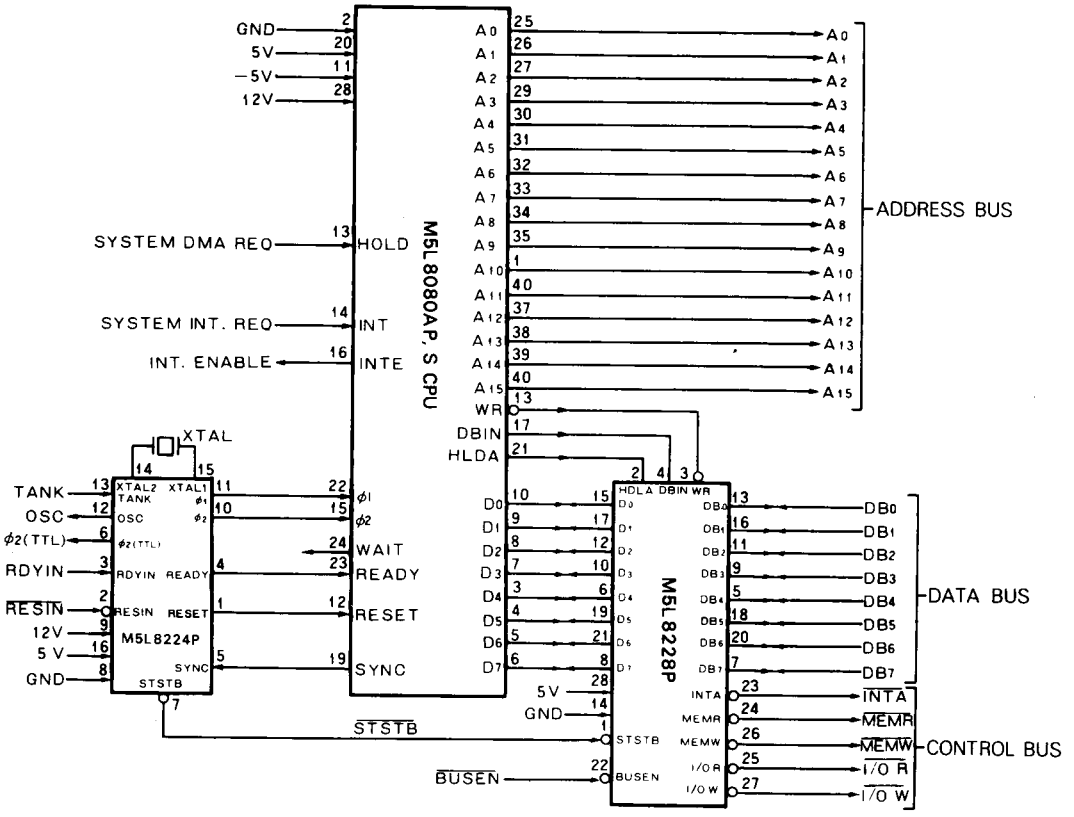
SYSTEM CONTROLLER AND BUS DRIVER FOR M5L 8080A P, S CPU

TYPICAL APPLICATION CIRCUIT



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