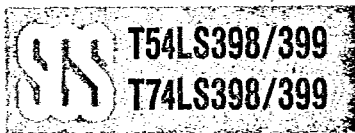


LOW POWER SCHOTTKY INTEGRATED CIRCUITS

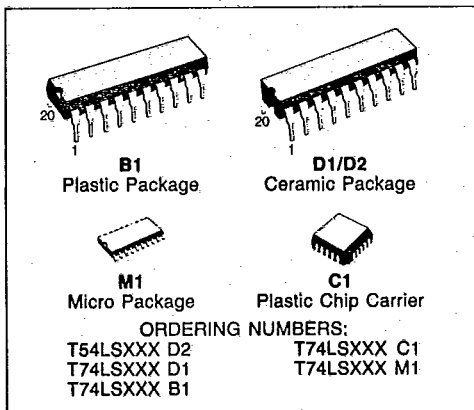


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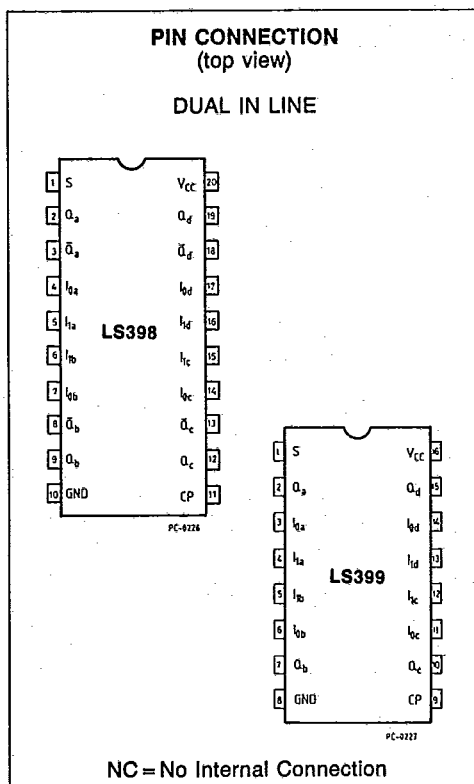
QUAD 2-PORT REGISTER

DESCRIPTION

The T54LS/T74LS398/399 are Quad 2-Port Registers. They are the logical equivalent of a quad 2-input multiplexer followed by a 4-bit edge-triggered register. Selection between two 4-bit input ports (data sources). The selected data is transferred to the output register on the LOW-to-HIGH transition of the Clock input. The T54LS/T74LS398 is composed of both Q and \bar{Q} inputs, while the T54LS/T74LS399 features only Q inputs.

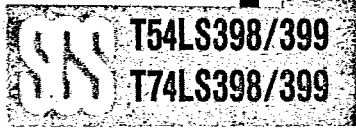


- FULLY POSITIVE EDGE-TRIGGERED OPERATION
- BOTH TRUE AND COMPLEMENTED OUTPUTS ON T54LS/T74LS398
- SELECT FROM TWO DATA SOURCES
- INPUT CLAMP DIODES LIMIT HIGH SPEED TERMINATION EFFECTS
- LS398 PRELIMINARY DATA

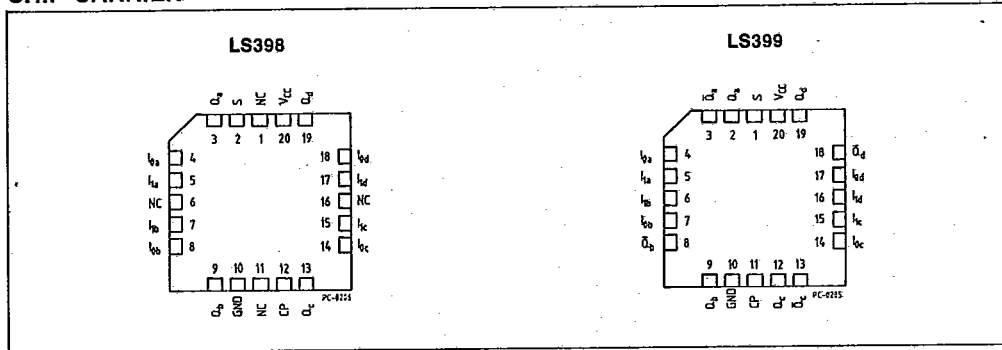


PIN NAMES

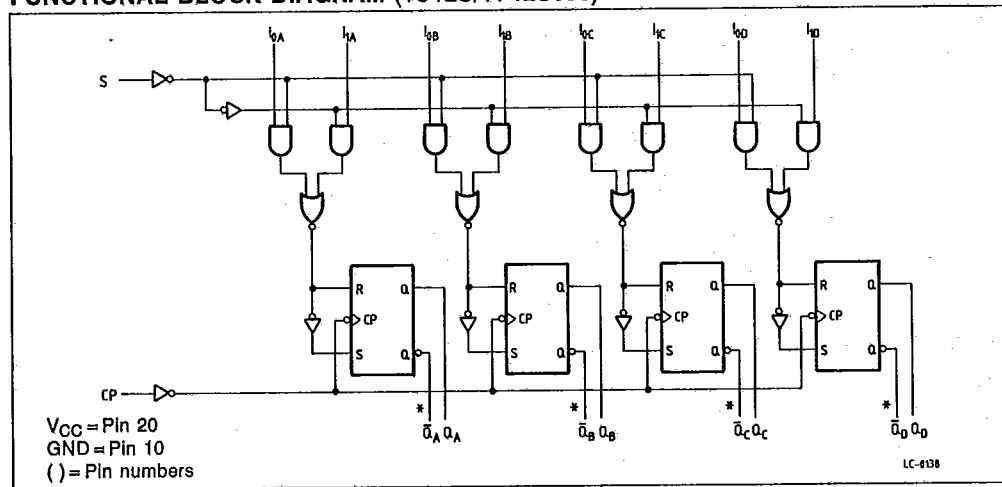
| | |
|-----------------------|--------------------------------------|
| S | Common Select Input |
| CP | Clock (Active HIGH going edge) Input |
| $I_{0a}-I_{0d}$ | Data Input From Source 0 |
| $I_{1a}-I_{1d}$ | Data Input From Source 1 |
| Q_a-Q_d | Register True Outputs |
| $\bar{Q}_a-\bar{Q}_d$ | Register Complementary Outputs |



CHIP CARRIER



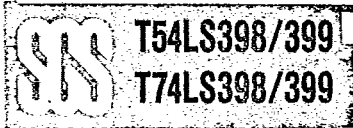
FUNCTIONAL BLOCK DIAGRAM (T54LS/T74LS398)



FUNCTIONAL DESCRIPTION

These high speed Quad 2-Port Registers select four bits of data from two sources (Port) under the control of a Common Select Input (S). The 4-bit Output Register where selected data are transferred is synchronous with the LOW-to-HIGH transition of the Clock input (CP). The 4-bit RS type output re-

gister is fully edge-triggered. Predictable operation is assured if Data inputs (I) and select inputs (S) are kept stable only a set-up time prior to and hold time after the LOW-to-HIGH transition of the Clock input. Both and Q inputs are available in the LS398.



TRUTH TABLE

| INPUTS | | | OUTPUTS | |
|--------|----------------|----------------|---------|----|
| S | I ₀ | I ₁ | Q | Q* |
| l | l | X | L | H |
| l | h | X | H | L |
| h | X | l | L | H |
| h | X | h | H | L |

* T54LS/T74LS398 only

L=LOW Voltage Level

H=HIGH Voltage Level

X=Don't Care

l=LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition

h=HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition

ABSOLUTE MAXIMUM RATINGS

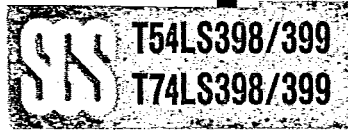
| Symbol | Parameter | Value | Unit |
|-----------------|-----------------------------------|------------|------|
| V _{CC} | Supply Voltage | -0.5 to 7 | V |
| V _I | Input Voltage, Applied to Input | -0.5 to 15 | V |
| V _O | Output Voltage, Applied to Output | 0 to 10 | V |
| I _I | Input Current, Into Inputs | -30 to 5 | mA |
| I _O | Output Current, Into Outputs | 50 | mA |

Stresses in excess of those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions in excess of those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

GUARANTEED OPERATING RANGES

| Part Numbers | Supply Voltage | | | Temperature |
|----------------|----------------|-------|--------|-----------------|
| | Min | Typ | Max | |
| T54LS398/399D2 | 4.5 V | 5.0 V | 5.5 V | -55°C to +125°C |
| T74LS398/399XX | 4.75 V | 5.0 V | 5.25 V | 0°C to +70°C |

XX=package type.



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

| Symbol | Parameter | Limits | | | Test Conditions (Note 1) | Units |
|-----------------|--|--------|-------|-----------|--|----------|
| | | Min. | Typ. | Max. | | |
| V _{IH} | Input HIGH Voltage | 2.0 | | | Guaranteed input HIGH Voltage for all Inputs | V |
| V _{IL} | Input LOW Voltage | 54 | | 0.7 | Guaranteed input LOW Voltage for all Inputs | V |
| | | 74 | | 0.8 | | |
| V _{CD} | Input Clamp Diode Voltage | | -0.65 | -1.5 | V _{CC} = MIN, I _{IN} = -18mA | V |
| V _{OH} | Output HIGH Voltage | 54 | 2.5 | 3.5 | V _{CC} = MIN, I _{OH} = -400mA, V _{IN} = V _{IH} or V _{IL} per Truth Table | V |
| | | 74 | 2.7 | 3.5 | | |
| V _{OL} | Output LOW Voltage | 54,74 | 0.25 | 0.4 | I _{OL} = 4.0mA V _{CC} = MIN, V _{IN} = V _{IH} or V _{IL} per Truth Table I _{OL} = 8.0mA | V |
| | | 74 | 0.35 | 0.5 | | |
| I _{IH} | Input HIGH Current | | | 20 0.1 | V _{CC} = MAX, V _{IN} = 2.7V V _{CC} = MAX, V _{IN} = 7.0V | μA mA |
| I _{IL} | Input LOW Current | | | -0.4 | V _{CC} = MAX, V _{IN} = 0.4V | mA |
| I _{OS} | Output Short Circuit Current (Note 2) | -20 | | -100 | V _{CC} = MAX | mA |
| I _{CC} | Power Supply Current | | | 13 | V _{CC} = MAX | mA |

AC CHARACTERISTICS: T_A = 25°C

| Symbol | Parameter | Limits | | | Test Conditions | Units |
|--------------------------------------|---|--------|----------|----------|---|-------|
| | | Min. | Typ. | Max. | | |
| t _{PLH} t _{PHL} | Propagation Delay, Clock to Output Q | | 18 21 | 27 32 | V _{CC} = 5.0V C _L = 15pF | ns |

Notes:

- 1) For conditions shown as MIN or MAX, use the appropriate value specified under guaranteed operating ranges.
- 2) Not more than one output should be shorted at a time.
- 3) Typical values are at V_{CC} = 5.0V, T_A = 25°C

AC SET-UP REQUIREMENTS: T_A = 25°C

| Symbol | Parameter | Limits | | | Test Conditions | Units |
|----------------|----------------------|--------|------|------|------------------------|-------|
| | | Min. | Typ. | Max. | | |
| t _w | Clock Pulse Width | 20 | | | V _{CC} = 5.0V | ns |
| t _s | Data Set-up Time | 25 | | | | ns |
| t _a | Select Set-up Time | 45 | | | | ns |
| t _h | Hold Time, Any Input | 0 | | | | ns |

DEFINITION OF TERMS:

SET-UP TIME (t_s) - is defined as the minimum time required for the correct logic level to be present at the logic input prior to the clock transition from LOW to HIGH in order to be recognized and transferred to the outputs.

HOLD TIME (t_h) - is defined as the minimum time following the clock transition from LOW to HIGH that the logic level must be maintained at the input in order to ensure continued recognition. A negative HOLD TIME indicates that the correct logic level may be released prior to the clock transition from LOW to HIGH and still be recognized.



T54LS398/399
T74LS398/399

AC WAVEFORMS

Fig. 1

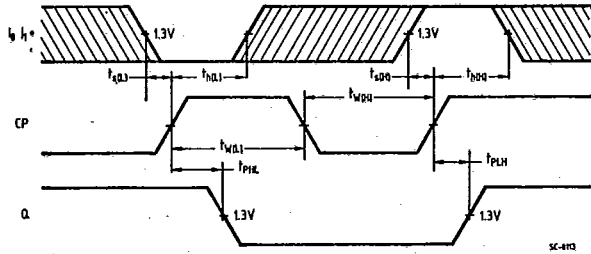


Fig. 2

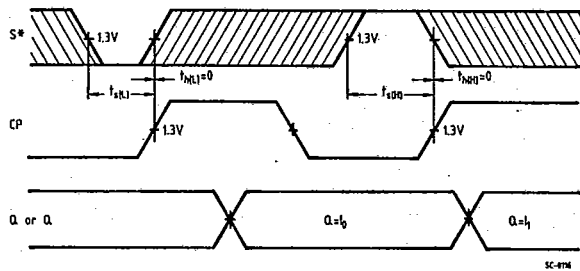
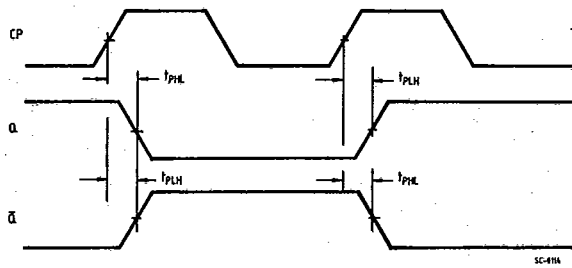
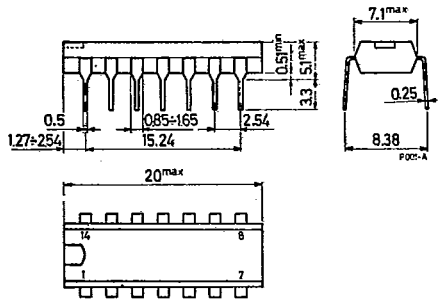
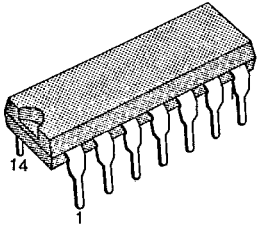


Fig. 3

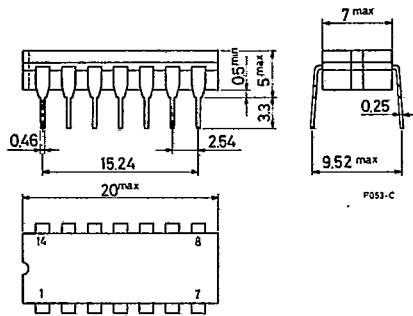
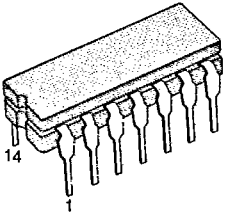


* The shaded areas indicate when the input is permitted to change for predictable output performance.

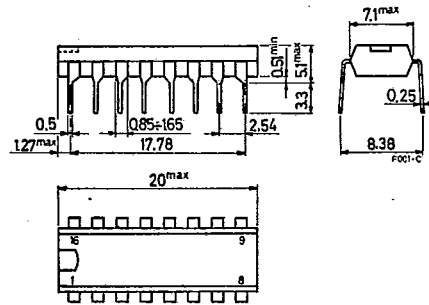
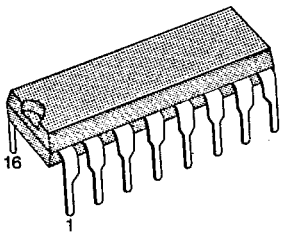
14-LEAD PLASTIC DIP



14-LEAD CERAMIC DIP



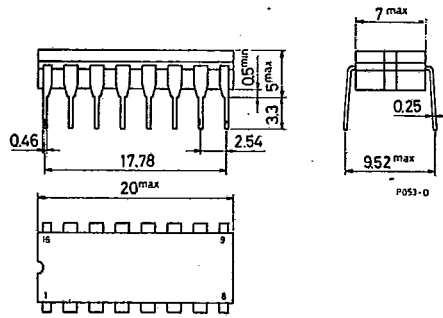
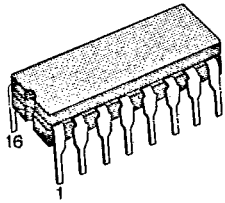
16-LEAD PLASTIC DIP



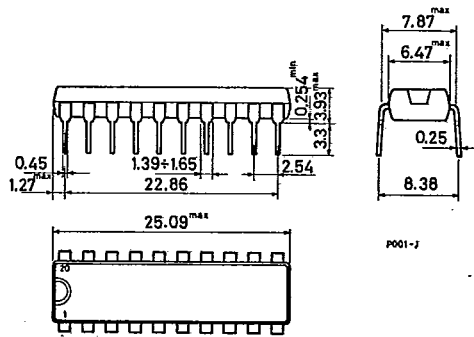
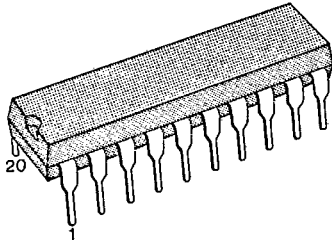
Packages

67C 16545 D T-90-20

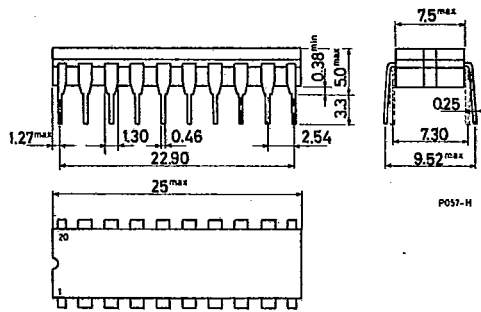
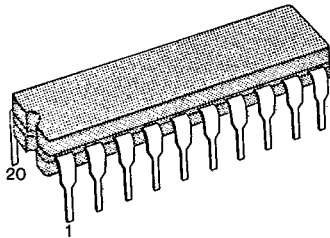
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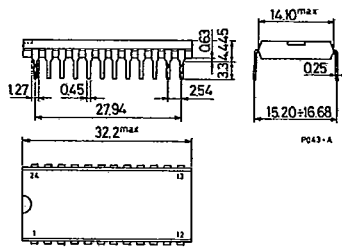
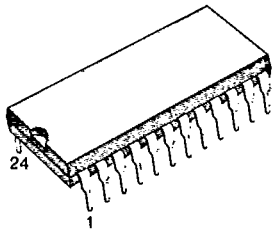
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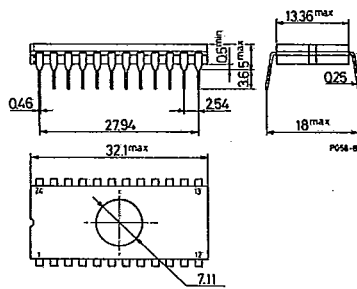
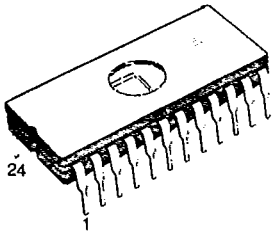
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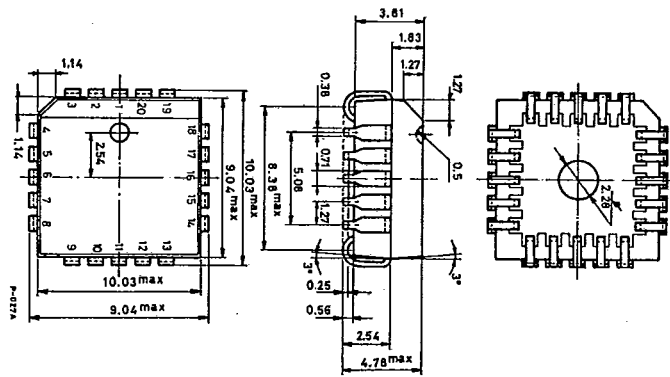
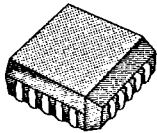
24-LEAD PLASTIC DIP



24-LEAD CERAMIC DIP



CHIP CARRIER 20 LEAD PLASTIC



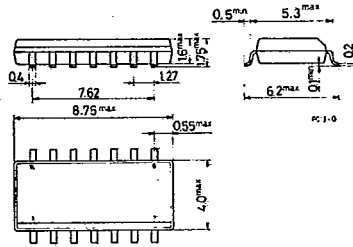
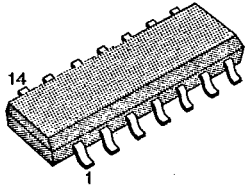
Packages

67C 16547

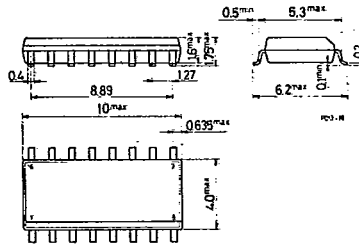
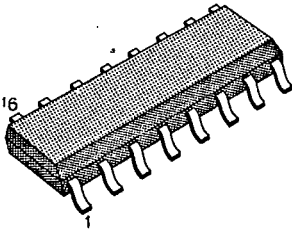
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T-90-20

14-LEAD PLASTIC DIP MICROPACKAGE



16-LEAD PLASTIC DIP MICROPACKAGE



NOTE: FOR 20-LEAD PLASTIC DIP MICROPACKAGE CONTACT SGS

Surface Mounted

67C 16548

D

T-90-20

One possible solution to the important problem of PWB minimization, is that of using surface mounted components. Integrated circuits in SO (Small Outline) packages are made up of standard chips mounted in very small plastic packages. The advantages given by using these devices are:

PWB Reduction

This is by far the most important advantage since the reduction of PWB size varies from 40 to 60% in comparison with standard board types. (See page 584 for package dimensions.)

Assembly Cost Reduction

SO Devices require no preliminary operation prior to mounting and can therefore be easily utilized in fully automatic equipment.

Increasing Reliability

The following characteristics lead to a higher level of reliability with respect to their standard packaged counter parts:

- The mounting system is fully automatic
- PWB number and the interconnections between them are reduced when the same number of devices are used.
- The high density of components on the board makes it thermally much more stable.

Noise Reduction and Improved Frequency Response

The reduction of the length of the connecting wires between the leads and the silicon guarantees a more homogeneous propagation delay between the external pins, with respect to the standard type.

Assembly Without Board Holes

The devices are placed on the board and soldered. This technology permits a higher level of tolerance in the positioning (automatic) of the device. For the standard DIP types this must be done with great accuracy due to the insertion of the leads into their holes.

