

## CMOS 8-Input NOR/OR Gate

High-Voltage Types (20-Volt Rating)

■ CD4078B NOR/OR Gate provides the system designer with direct implementation of the positive-logic 8-input NOR and OR functions and supplements the existing family of CMOS gates.

The CD4078B types are supplied in 14-lead hermetic dual-in-line ceramic packages (F3A suffix), 14-lead dual-in-line plastic packages (E suffix), 14-lead small-outline packages (M, MT, M96, and NSR suffixes), and 14-lead thin shrink small-outline packages (PW and PWR suffixes).

Voltages referenced to $V_{SS}$ Terminal)	.....	-0.5V to +20V
INPUT VOLTAGE RANGE, ALL INPUTS	.....	-0.5V to $V_{DD}$ +0.5V
DC INPUT CURRENT, ANY ONE INPUT	.....	$\pm 10$ mA
POWER DISSIPATION PER PACKAGE ( $P_D$ ):		
For $T_A = -55^\circ\text{C}$ to $+100^\circ\text{C}$	.....	500mW
For $T_A = +100^\circ\text{C}$ to $+125^\circ\text{C}$	.....	Derate Linearity at 12mW/ $^\circ\text{C}$ to 200mW
DEVICE DISSIPATION PER OUTPUT TRANSISTOR		
FOR $T_A = \text{FULL PACKAGE-TEMPERATURE RANGE (All Package Types)}$	.....	100mW
OPERATING-TEMPERATURE RANGE ( $T_A$ )	.....	$-55^\circ\text{C}$ to $+125^\circ\text{C}$
STORAGE TEMPERATURE RANGE ( $T_{stg}$ )	.....	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
LEAD TEMPERATURE (DURING SOLDERING):		
At distance $1/16 \pm 1/32$ inch ( $1.59 \pm 0.79$ mm) from case for 10s max	.....	$+265^\circ\text{C}$

**RECOMMENDED OPERATING CONDITIONS**  
For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges:

CHARACTERISTIC	Min.	Max.	Units
Supply-Voltage Range (For $T_A$ Full Package Temperature Range)	3	18	V

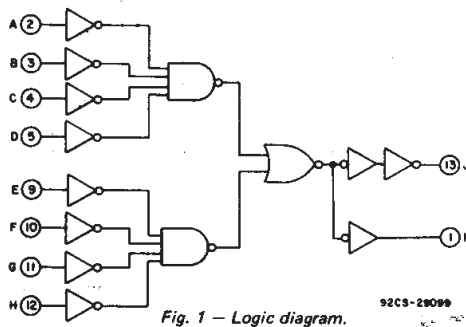


Fig. 1 - Logic diagram.

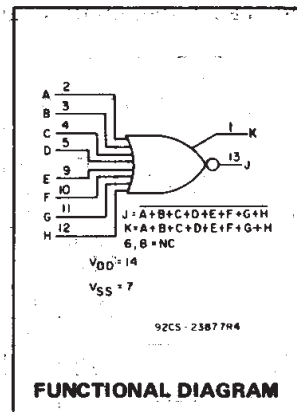
### DYNAMIC ELECTRICAL CHARACTERISTICS

At  $T_A = 25^\circ\text{C}$ ; Input  $t_r, t_f = 20$  ns,  $C_L = 50$  pF,  $R_L = 200$  k $\Omega$

CHARACTERISTIC	TEST CONDITIONS	LIMITS		UNITS	
		$V_{DD}$ VOLTS	TYP.		MAX.
Propagation Delay Time, $t_{PHL}, t_{PLH}$		5	150	300	ns
		10	75	150	
		15	55	110	
Transition Time, $t_{THL}, t_{TLH}$		5	100	200	ns
		10	50	100	
		15	40	80	
Input Capacitance, $C_{IN}$	Any Input		5	7.5	pF

### Features:

- Medium-Speed Operation:  
 $t_{PHL}, t_{PLH} = 75$  ns (typ.) at  $V_{DD} = 10$  V
- Buffered inputs and output
- 5-V, 10-V, and 15-V parametric ratings
- Standardized symmetrical output characteristics
- 100% tested for quiescent current at 20 V
- Maximum input current of  $1 \mu\text{A}$  at 18 V over full package-temperature range:  
100 nA at 18 V and  $25^\circ\text{C}$
- Noise margin (over full package-temperature range):  
1 V at  $V_{DD} = 5$  V  
2 V at  $V_{DD} = 10$  V 2.5 V at  $V_{DD} = 15$  V
- Meets all requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"



FUNCTIONAL DIAGRAM

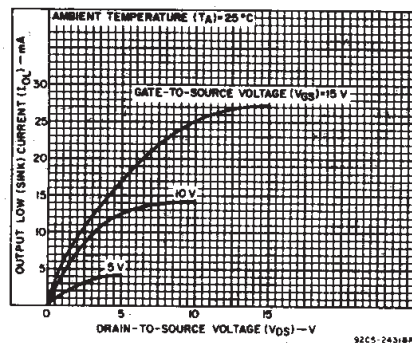


Fig. 2 - Typical output low (sink) current characteristics.

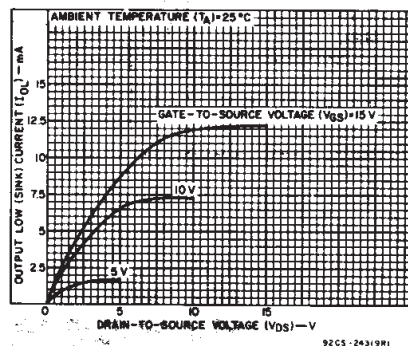


Fig. 3 - Minimum output low (sink) current characteristics.

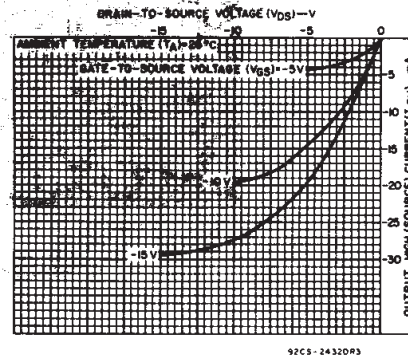


Fig. 4 - Typical output high (source) current characteristics.

# CD4078B Types

## STATIC ELECTRICAL CHARACTERISTICS

CHARACTERISTIC	CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)							UNITS
	V <sub>O</sub> (V)	V <sub>IN</sub> (V)	V <sub>DD</sub> (V)	-55	-40	+85	+125	+25			
								Min.	Typ.	Max.	
Quiescent Device Current, I <sub>DD</sub> Max.	-	0.5	5	0.25	0.25	7.5	7.5	-	0.01	0.25	μA
	-	0.10	10	0.5	0.5	15	15	-	0.01	0.5	
	-	0.15	15	1	1	30	30	-	0.01	1	
	-	0.20	20	5	5	150	150	-	0.02	5	
Output Low (Sink) Current, I <sub>OL</sub> Min.	0.4	0.5	5	0.64	0.61	0.42	0.36	0.51	1	mA	
	0.5	0.10	10	1.6	1.5	1.1	0.9	1.3	2.6		
	1.5	0.15	15	4.2	4	2.8	2.4	3.4	6.8		
Output High (Source) Current, I <sub>OH</sub> Min.	4.6	0.5	5	-0.64	-0.61	-0.42	-0.36	-0.51	-1	mA	
	2.5	0.5	5	-2	-1.8	-1.3	-1.15	-1.6	-3.2		
	9.5	0.10	10	-1.6	-1.5	-1.1	-0.9	-1.3	-2.6		
	13.5	0.15	15	-4.2	-4	-2.8	-2.4	-3.4	-6.8		
Output Voltage: Low Level, V <sub>OL</sub> Max.	-	0.5	5	0.05				0	0.05	V	
	-	0.10	10	0.05				0	0.05		
	-	0.15	15	0.05				0	0.05		
Output Voltage: High Level, V <sub>OH</sub> Min.	-	0.5	5	4.95				4.95	5	V	
	-	0.10	10	9.95				9.95	10		
	-	0.15	15	14.95				14.95	15		
Input Low Voltage, V <sub>IL</sub> Max.	0.5, 4.5	-	5	1.5				-	-	1.5	V
	1.9	-	10	3				-	-	3	
	1.5, 13.5	-	15	4				-	-	4	
Input High Voltage, V <sub>IH</sub> Min.	0.5, 4.5	-	5	3.5				3.5	-	-	V
	1.9	-	10	7				7	-	-	
	1.5, 13.5	-	15	11				11	-	-	
Input Current I <sub>IN</sub> Max.		0.18	18	±0.1	±0.1	±1	±1	-	±10 <sup>-5</sup>	±0.1	μA

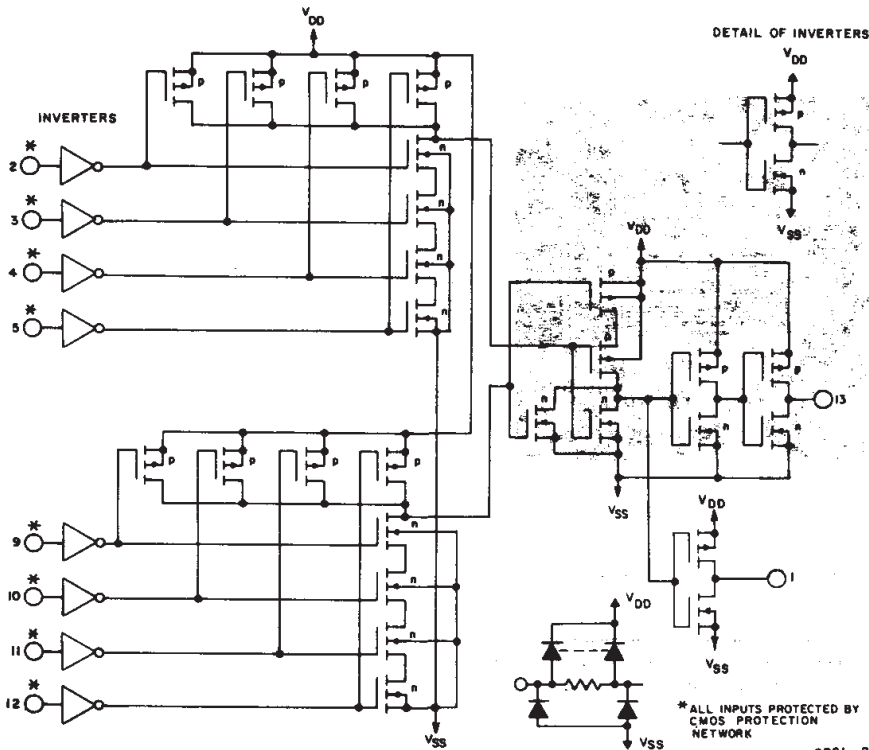
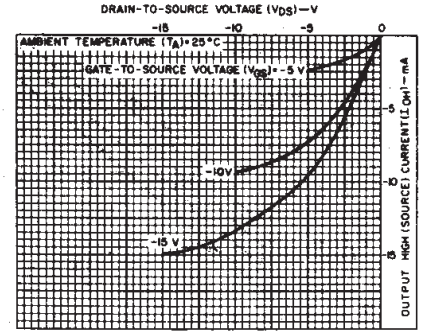


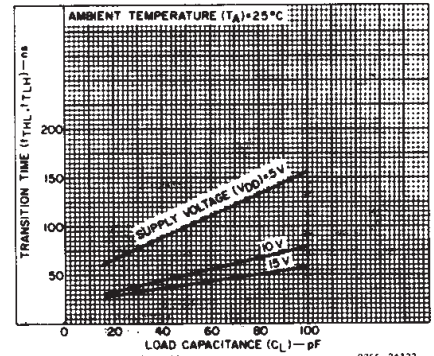
Fig. 8 - Schematic diagram.

92CL-29098



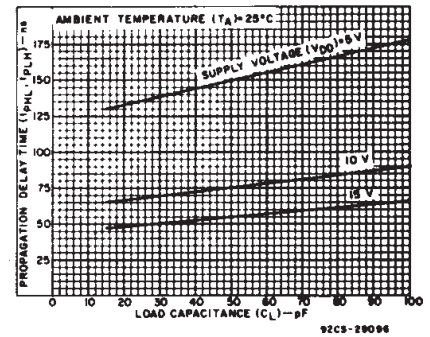
92CS-24321R2

Fig. 5 - Minimum output high (source) current characteristics.



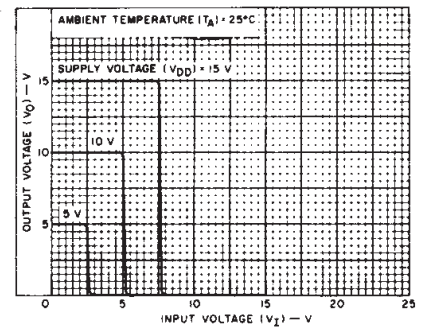
92CS-24322

Fig. 6 - Typical transition time as a function of load capacitance.



92CS-29096

Fig. 7 - Typical propagation delay time as a function of load capacitance.



92CS-28904

Fig. 9 - Typical voltage transfer characteristics (NOR output).

3  
COMMERCIAL CMOS  
HIGH VOLTAGE ICs

# CD4078B Types

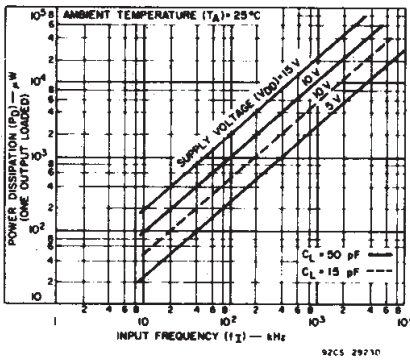


Fig. 10 – Typical dynamic power dissipation as a function of frequency.

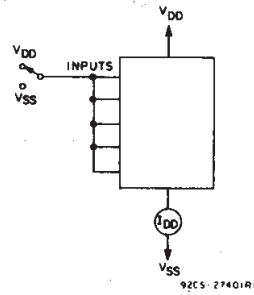


Fig. 11 – Quiescent-device-current test circuit.

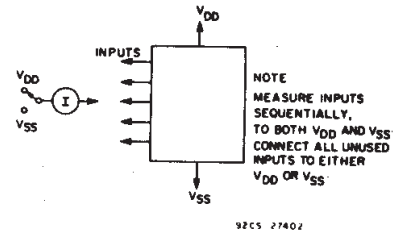


Fig. 12 – Input current test circuit.

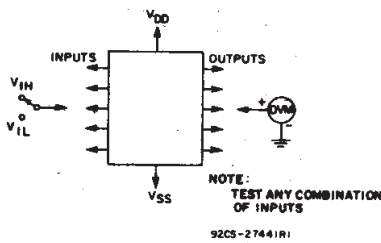


Fig. 13 – Input-voltage test circuit.

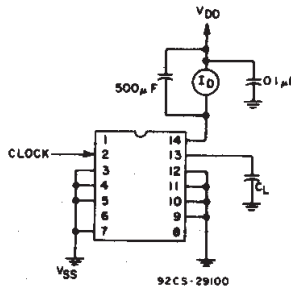
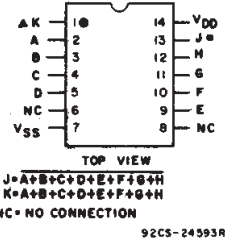
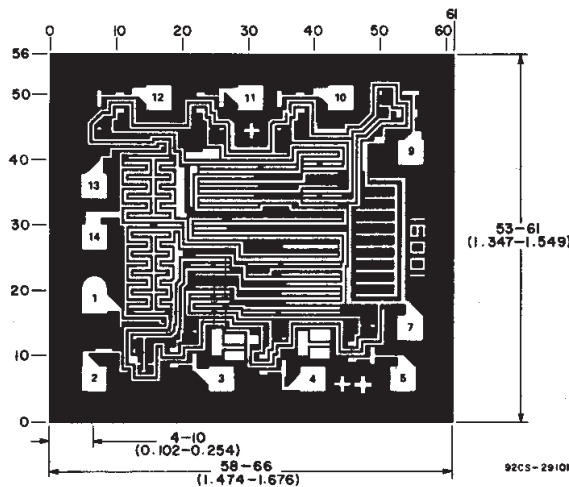


Fig. 14 – Dynamic power dissipation test circuit.



## TERMINAL ASSIGNMENT



Dimensions and pad layout for CD4078BH.

Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduations are in mils ( $10^{-3}$  inch).

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**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
7704402CA	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
CD4078BE	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4078BEE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
CD4078BF	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
CD4078BF3A	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
CD4078BM	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4078BM96	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4078BM96E4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4078BM96G4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4078BME4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4078BMG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4078BMT	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4078BMTE4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4078BMTG4	ACTIVE	SOIC	D	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4078BNSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4078BNSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4078BPW	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4078BPWE4	ACTIVE	TSSOP	PW	14	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4078BPWR	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
CD4078BPWRE4	ACTIVE	TSSOP	PW	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered

at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

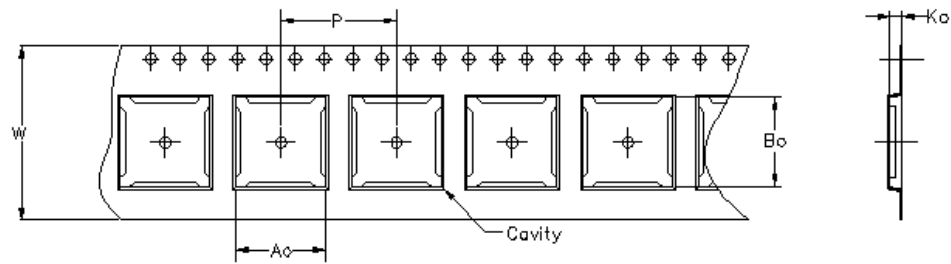
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

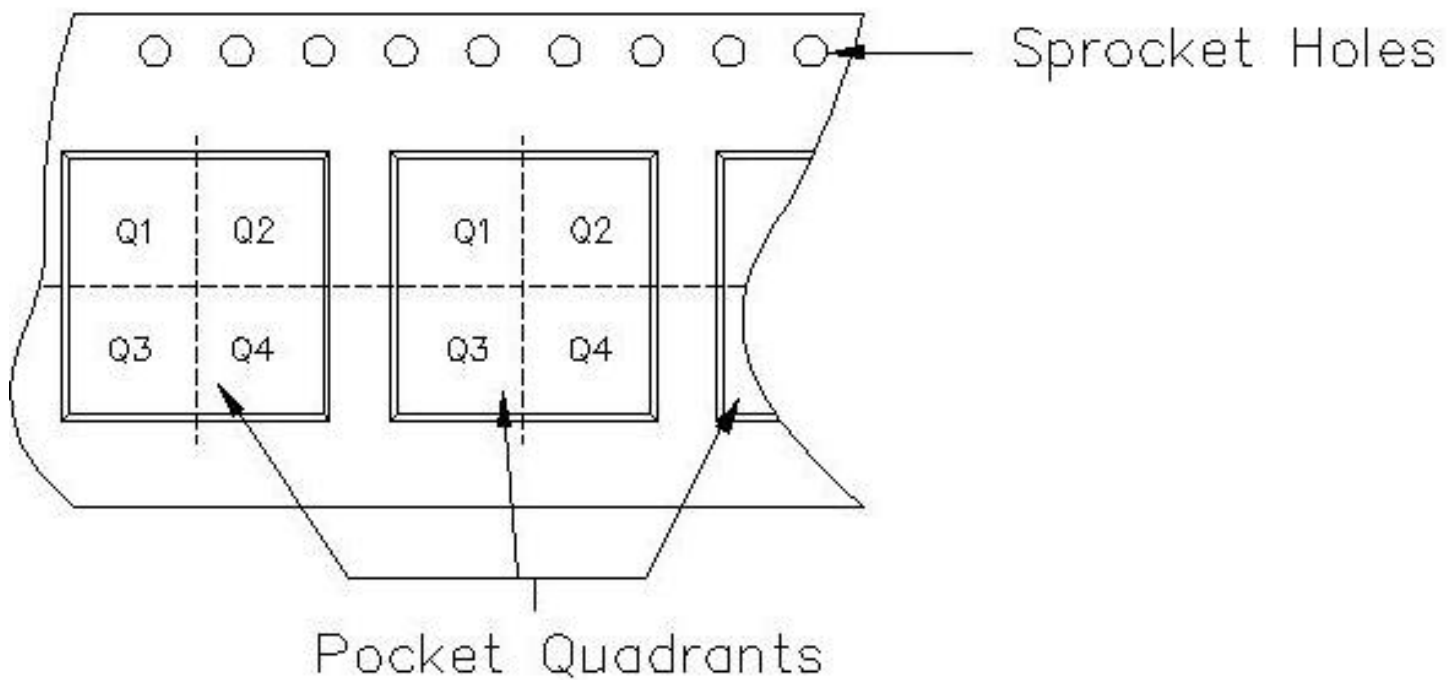
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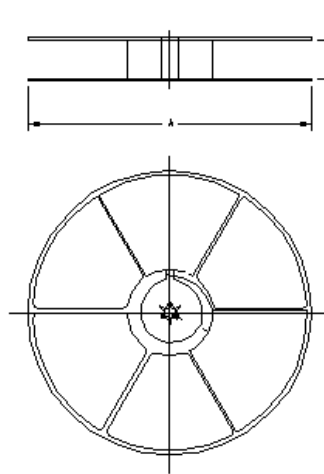
Carrier tape design is defined largely by the component length, width, and thickness.

$A_o$ = Dimension designed to accommodate the component width.
$B_o$ = Dimension designed to accommodate the component length.
$K_o$ = Dimension designed to accommodate the component thickness.
$W$ = Overall width of the carrier tape.
$P$ = Pitch between successive cavity centers.



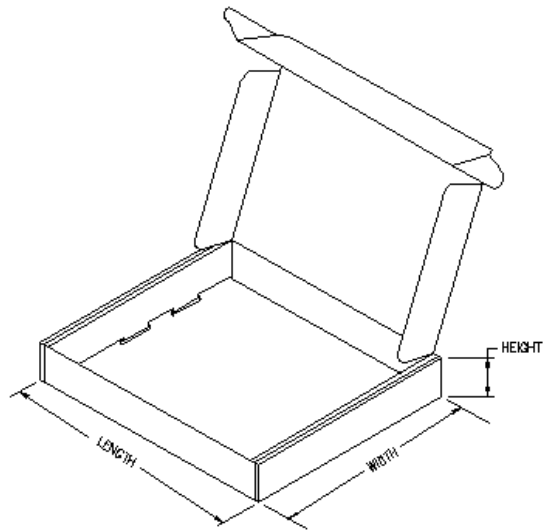
**TAPE AND REEL INFORMATION**

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD4078BM96	D	14	MLA	330	16	6.5	9.0	2.1	8	16	Q1
CD4078BNSR	NS	14	MLA	330	16	8.2	10.5	2.5	12	16	Q1
CD4078BPWR	PW	14	MLA	330	12	7.0	5.6	1.6	8	12	Q1



**TAPE AND REEL BOX INFORMATION**

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
CD4078BM96	D	14	MLA	333.2	333.2	28.58
CD4078BNSR	NS	14	MLA	333.2	333.2	28.58
CD4078BPWR	PW	14	MLA	338.1	340.5	20.64



# J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package is hermetically sealed with a ceramic lid using glass frit.
  - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G14)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
  - $\triangle D$  Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
  - E. Reference JEDEC MS-012 variation AB.

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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